Welcome to the world of JUNCTIONLESS NANOWIRE FETs!

Isabelle FERAIN

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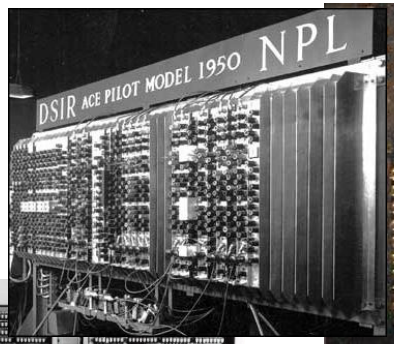
University College Cork

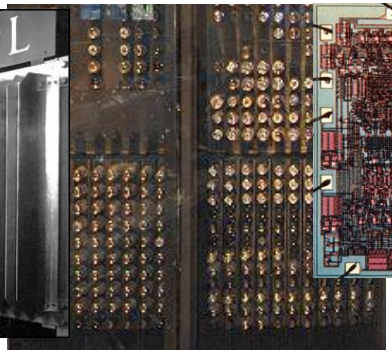
Ireland's EU Structural Funds Programmes 2007 - 2013

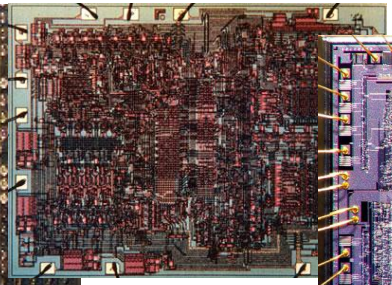
Co-funded by the Irish Government and the European Union

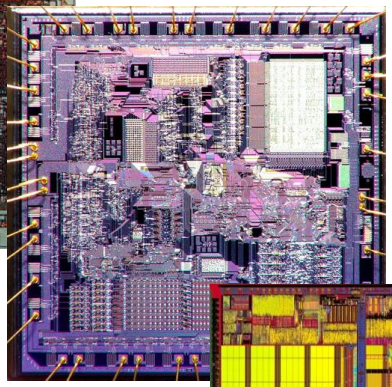
EUROPEAN REGIONAL DEVELOPMENT FUND

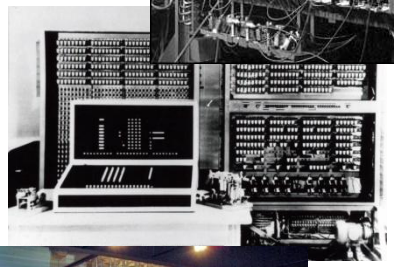
Dimensions scaling

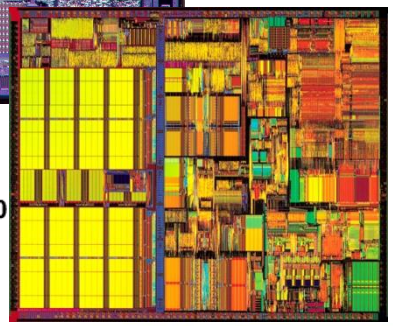


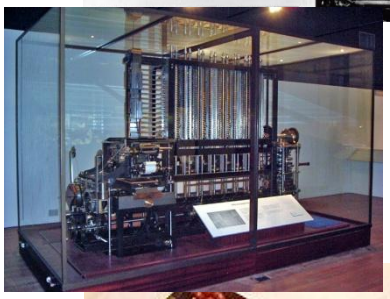


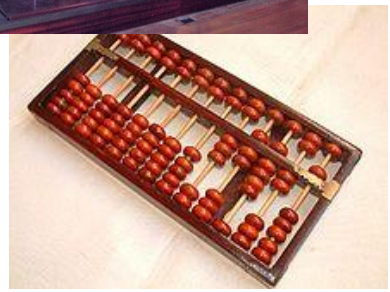


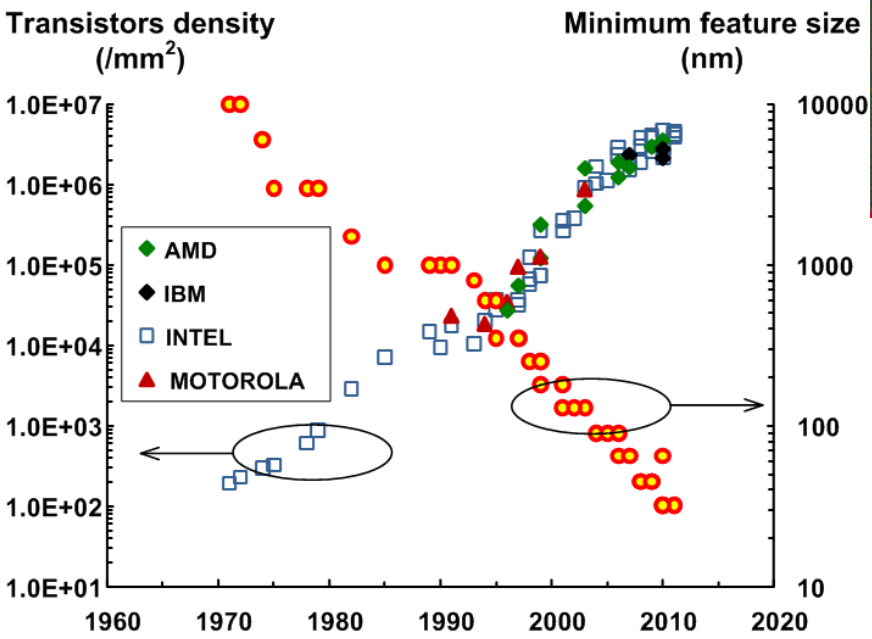


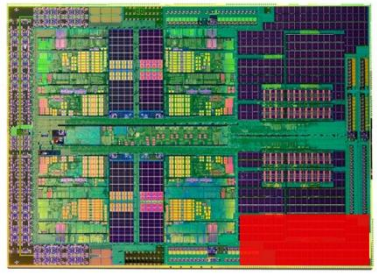












Voltage scaling

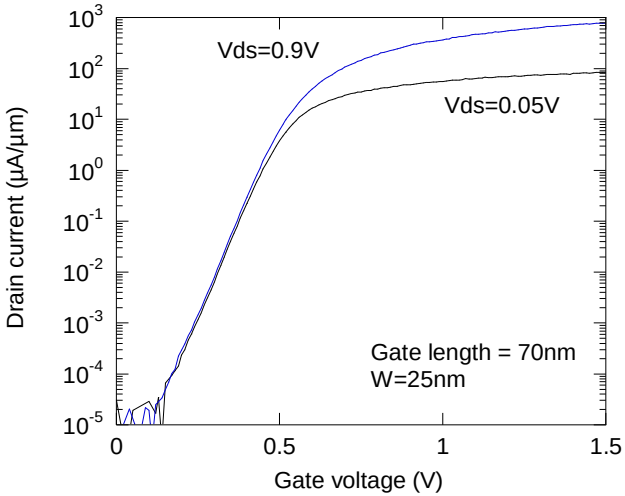
- Dynamic power dissipation in present CMOS circuits at frequency, *f*, supply voltage, V_{DD} and load capacitance C_{load} can be described by:

$$P_{dynamic} = C_{load} \cdot V_{dd}^{2} \cdot f_{cycle}$$

- Any reduction of power consumption thus requires to *reduce supply voltage*

- V_{dd} scaling is
  - set by the threshold voltage of transistors
  - dependent on the inverse sub-threshold slope (kT/q)
  - limited by short-channel effects

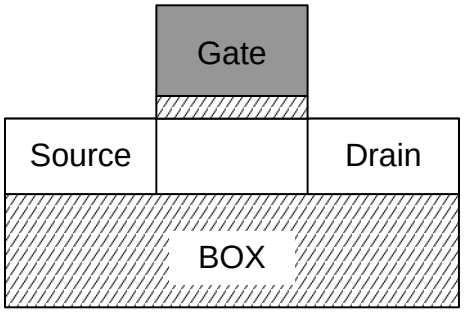
→ *Enhanced coupling between gate and channel*

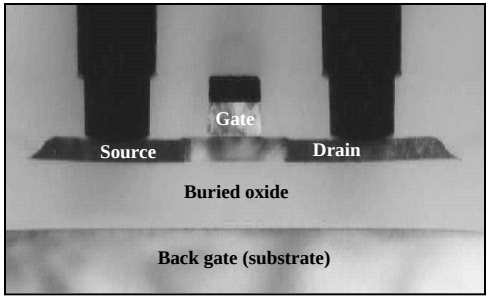


Courtesy:
Prof. Gerard Ghibaudo (IMEP)

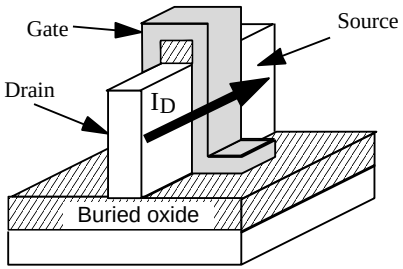
Enhanced Electrostatic Control

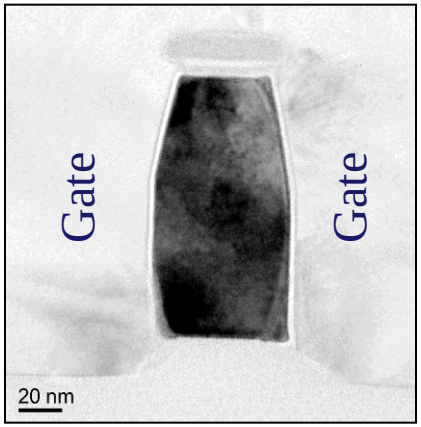
"1 Gate"



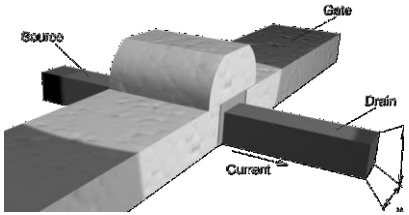


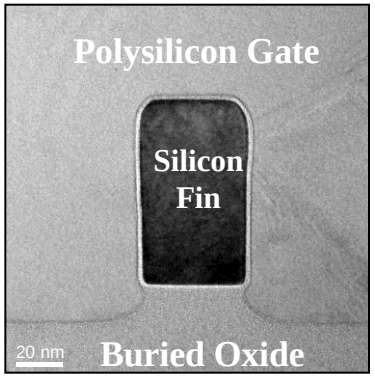
"2 Gates"



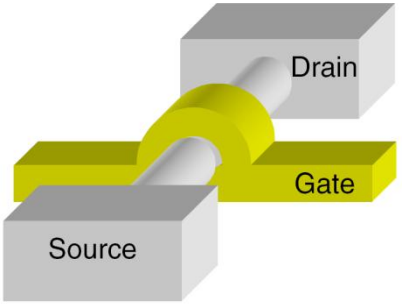


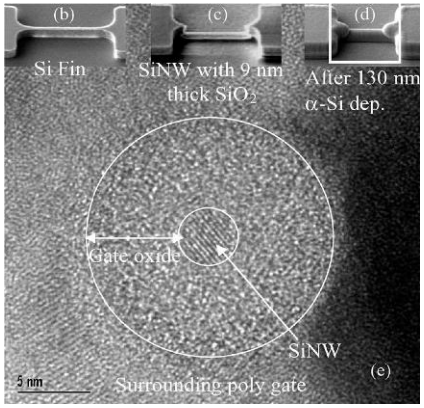
"3 Gates"





"Gate-all-Around"





Does it look too good to be true?

- Improved L_g scalability
- Almost ideal sub-threshold slope (60mV/dec) at RT
- Low drain-to-source current (I_{OFF})

- Drive current I_{ON}
  - crystal orientation dependence
  - High nano-wire pitch density
- Source/Drain resistance R_{sd}
  - SEG / Layout optimization needed

Critical Dimensions
- Gate length
- Gate oxide thickness
- Junction Depth

→

Critical Dimensions
- Nano-wire width
- Junction abruptness

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DEVICE STRUCTURE

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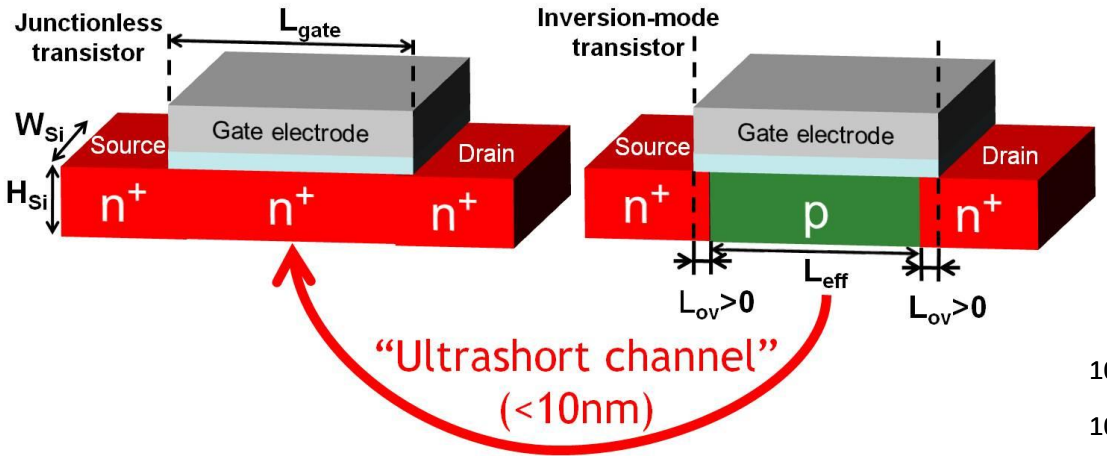
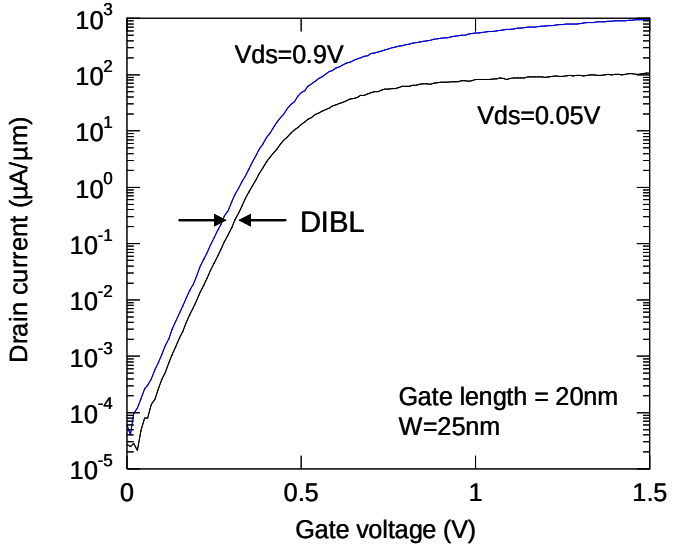
Device Structure (1/2)

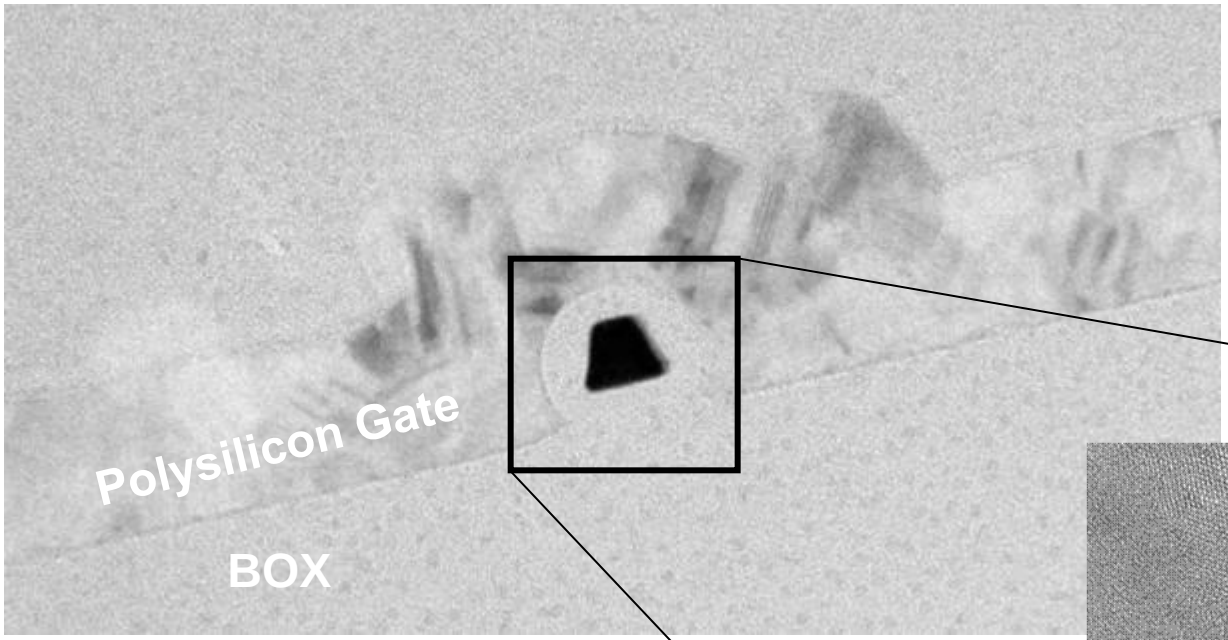


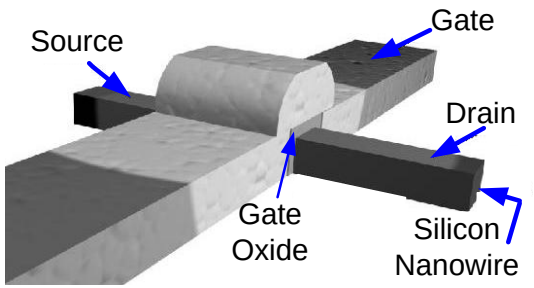
Hooray!!
No need for source & drain engineering anymore!

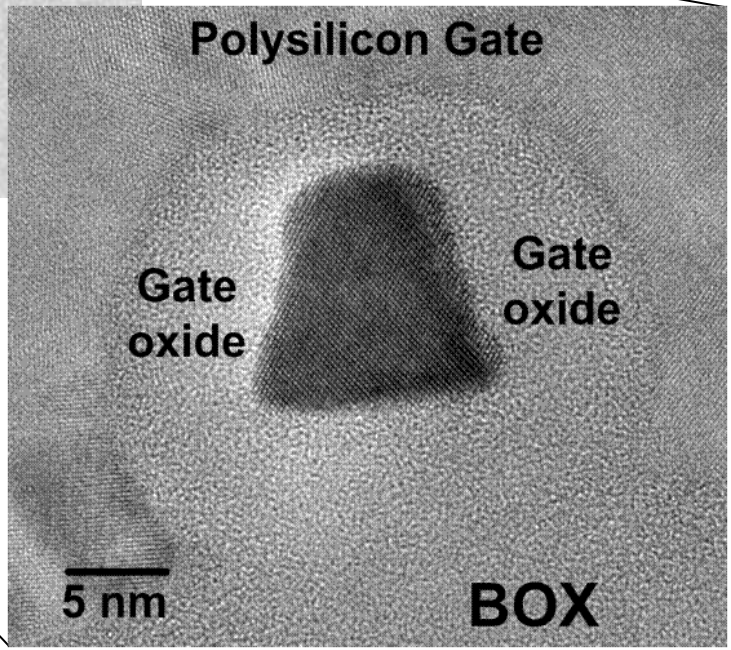


J.-P. Colinge et al., *Nanowire transistors without junctions*, Nature Nanotechnology, Vol. 5, No. 3, pp. 225-229, 2010.

Device structure (2/2)







The cross-section of the channel must be small enough so that the gate can deplete the heavily doped channel entirely (OFF state)

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Junctionless nanowire transistors

CONDUCTION MECHANISM

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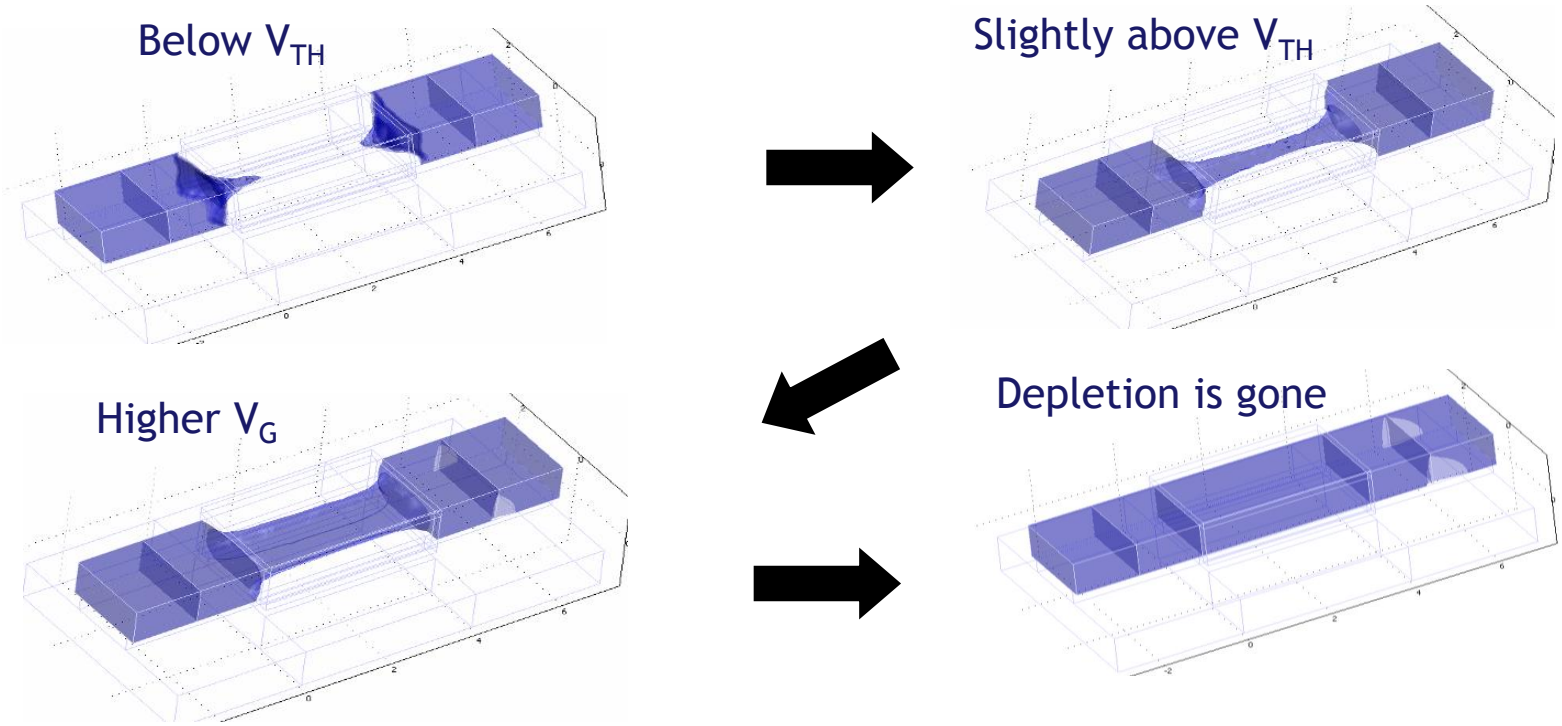
Conduction mechanism (1/4)

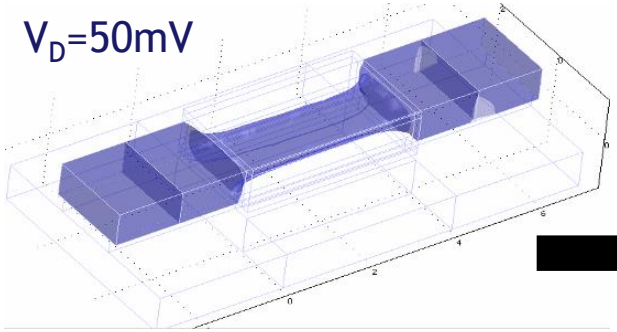
Electrostatic pinch-off:

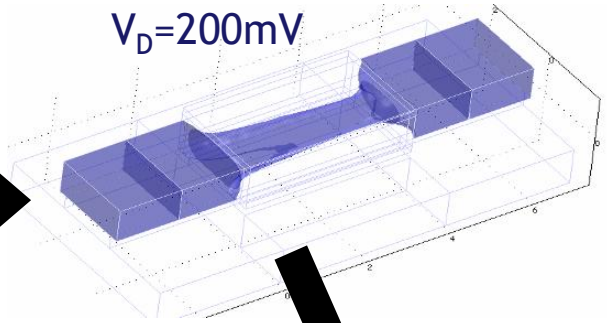
The cross section is small enough for the channel region to be depleted (V_D=50mV, N_d>5e18/cm^3)

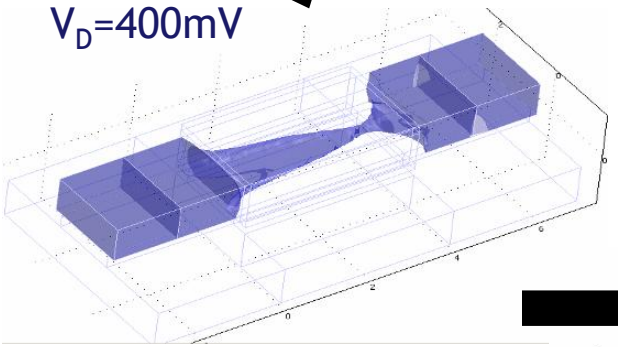


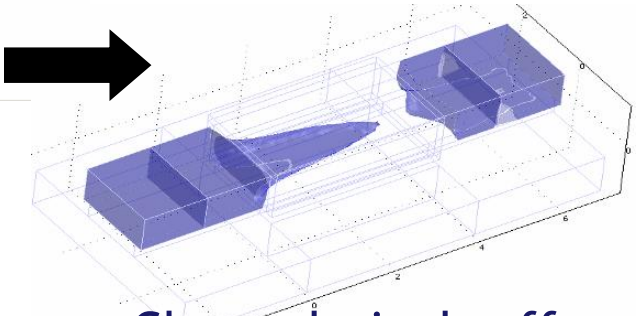
Conduction mechanism (2/4)

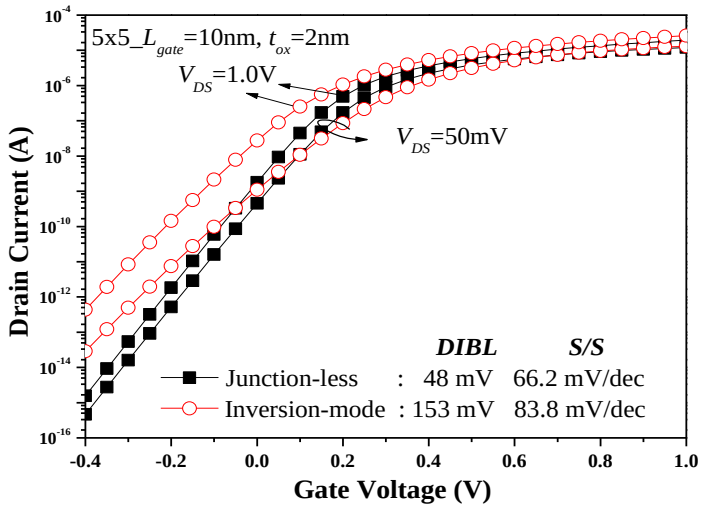
$V_G > V_{TH}$





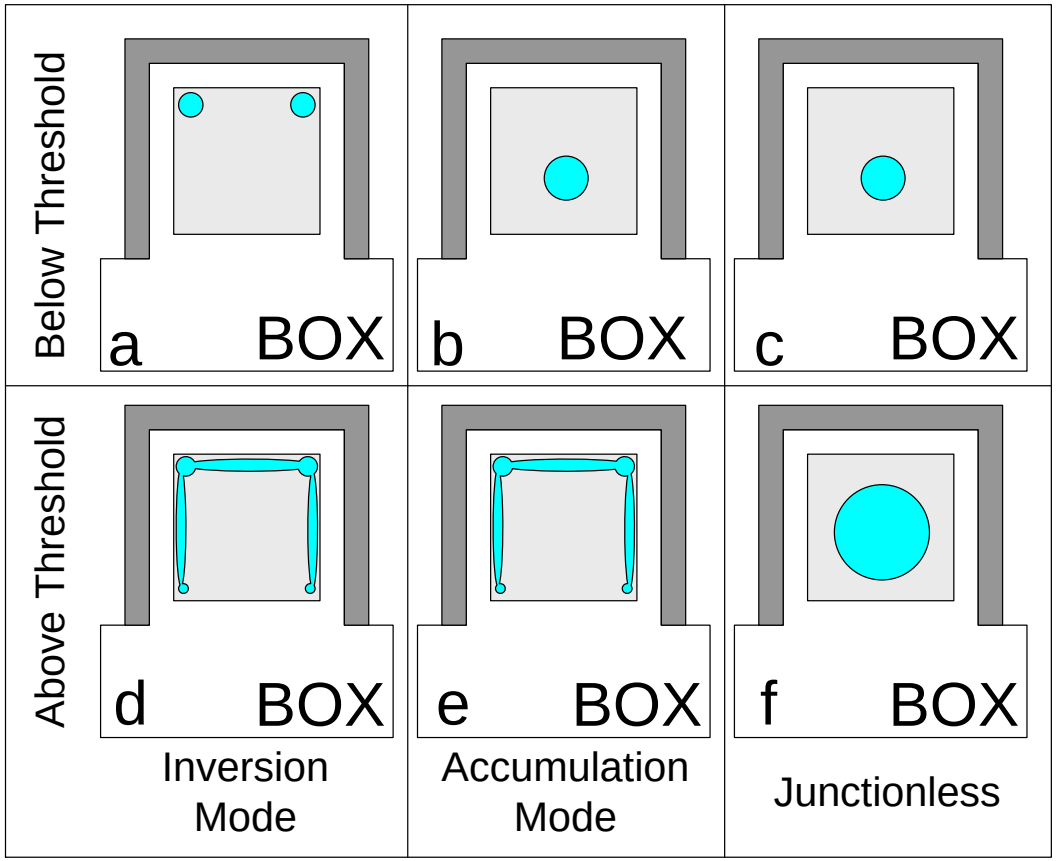






Channel pinch-off

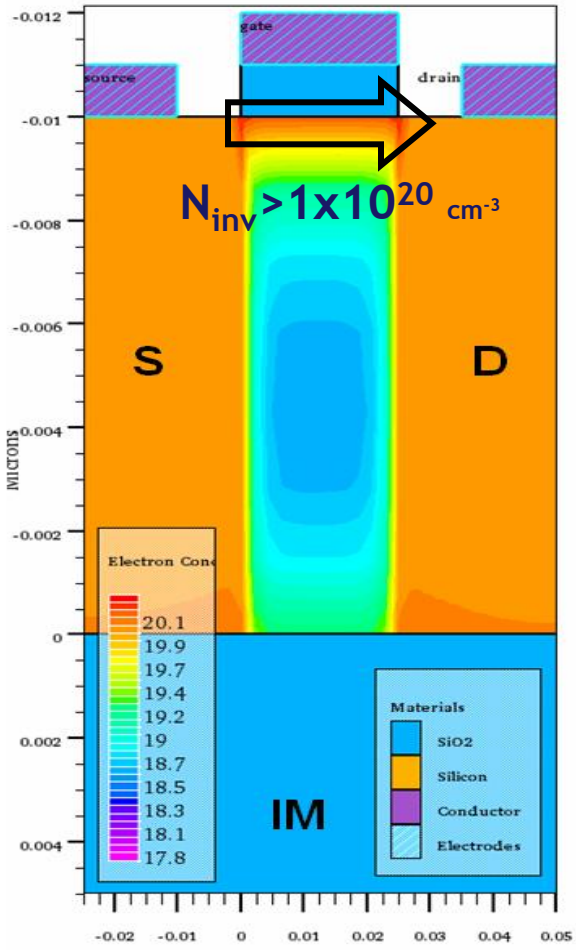
Conduction mechanism (3/4)

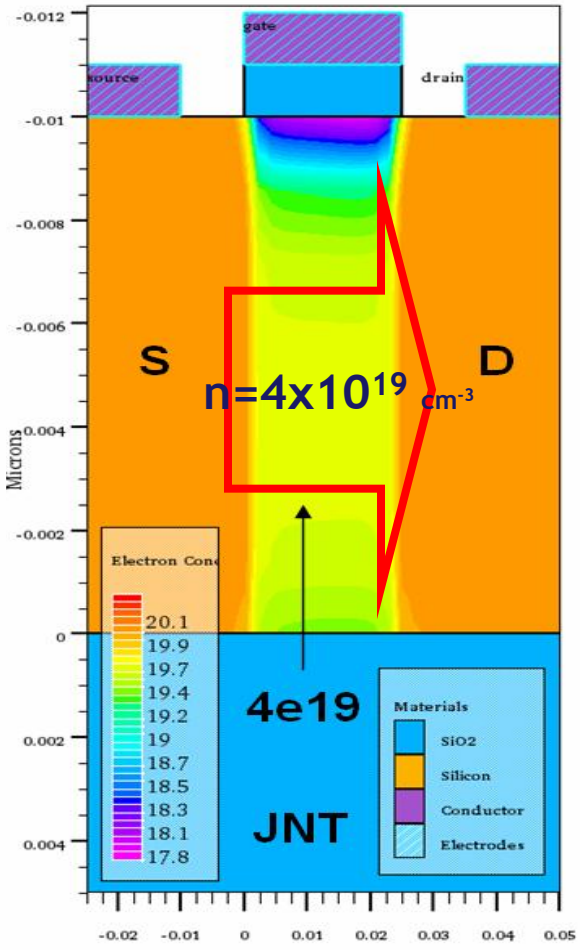


Conduction mechanism (4/4)

Channel in Multigate FETs @ V_G= V_G =1V

N^+PN^+ Inversion Mode





$N^+N^+N^+$ Junctionless N_D=1x10^{19}cm^{-3}

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MOBILITY

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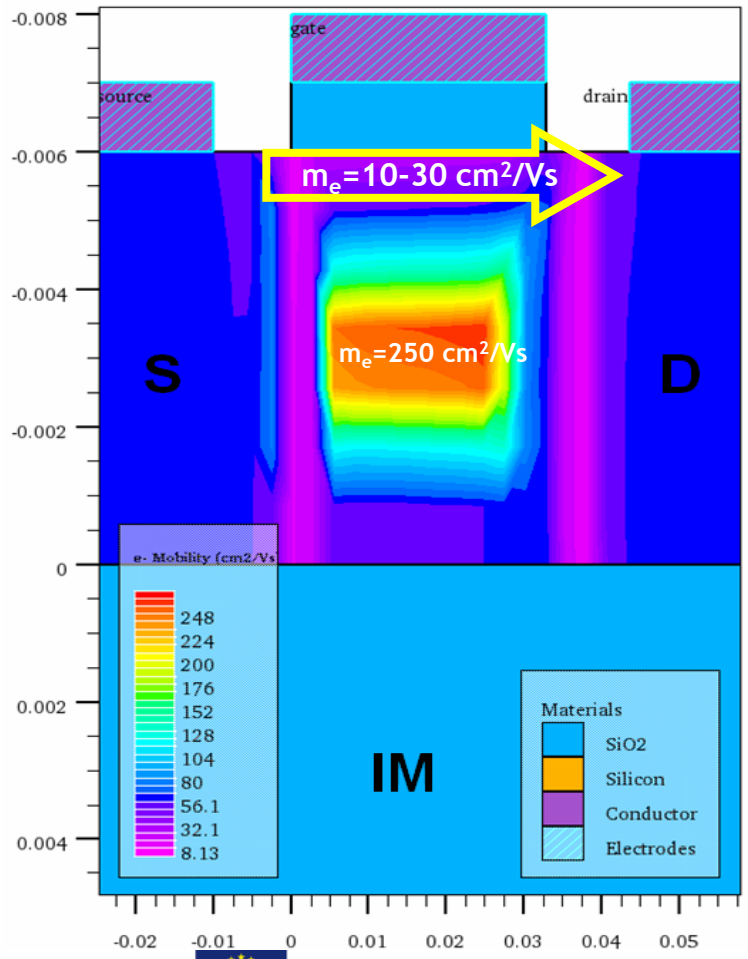
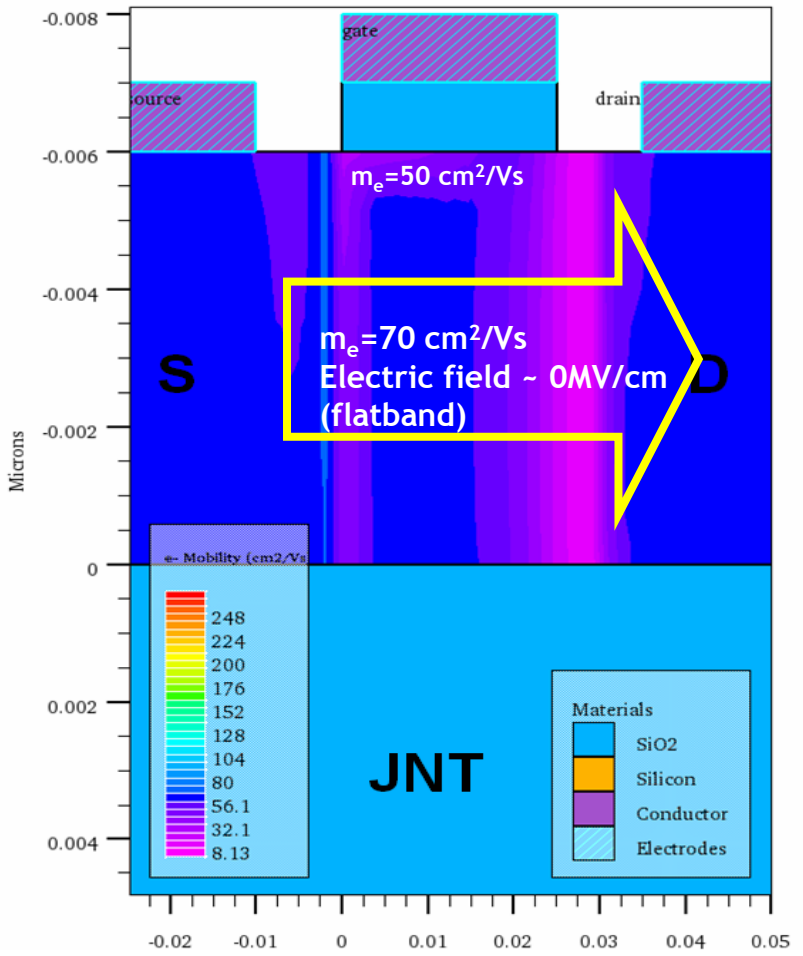
Electron Mobility (1/2)

$V_G = V_G = 1V$

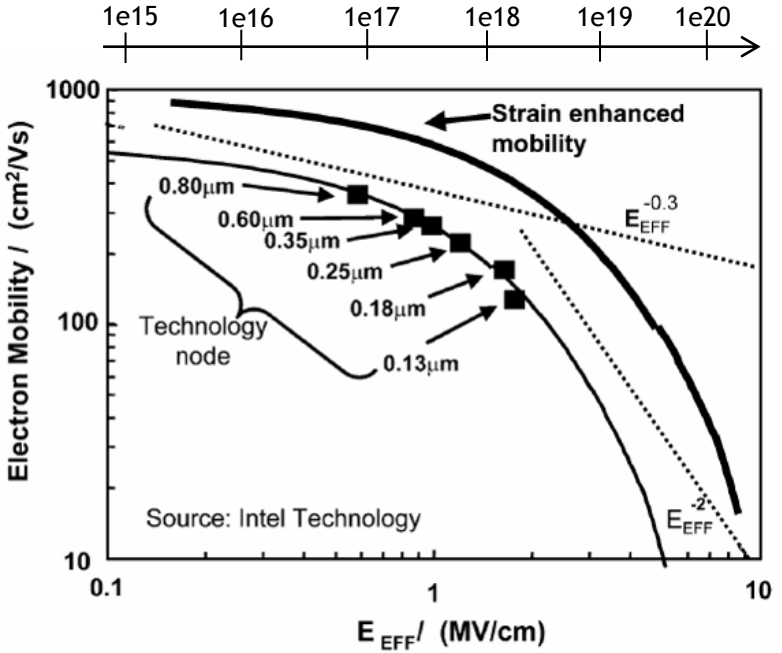
N^+PN^+ Inversion Mode

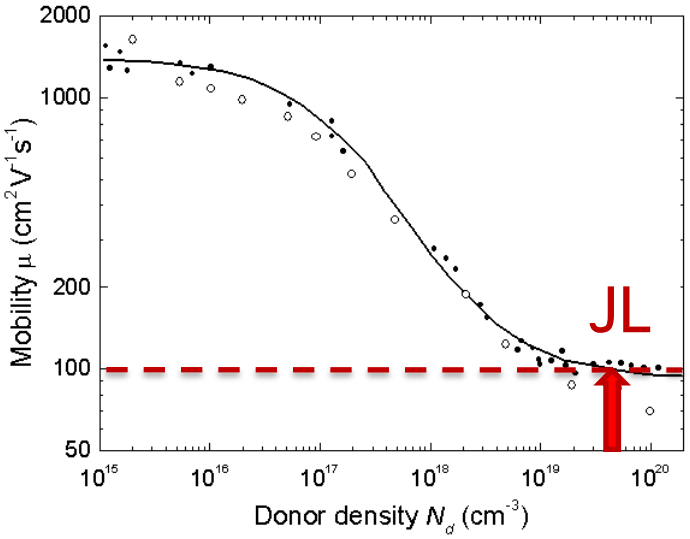


$N^+N^+N^+$ Junctionless $N_D=1x10^{19}cm^{-3}$



Electron Mobility (2/2)





- L_g and EOT scaling → increased E_{eff} in the channel → µ decreases
- Without strain technology the channel mobility in IM/AM FETs would be = or lower than in heavily doped Si

- Thompson S.E. et al., A 90-nm logic technology featuring strained-silicon, IEEE Transactions on Electron Devices, vol.51, 11 (2004) 1790-1797.
- Jacoboni, C. et al., *A review of some charge transport properties of silicon*, Solid State Electron. 20, issue 2(1977) 77-89.
- J.P.-Colinge et al., *Reduced electric field in junctionless transistors*, Applied Physics Letters 96 (2010) 073510.

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PROCESS INDUCED-VARIABILITY

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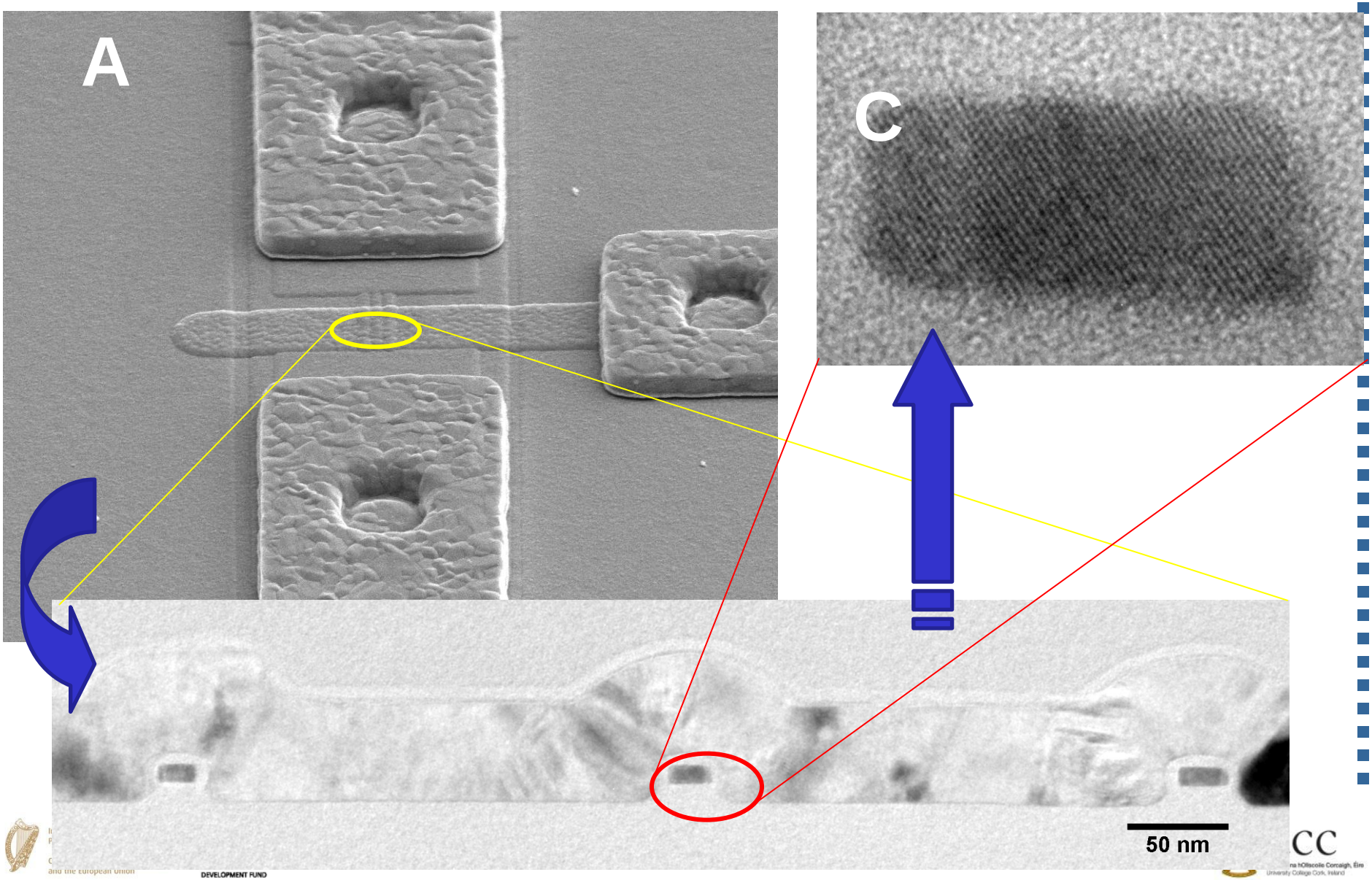
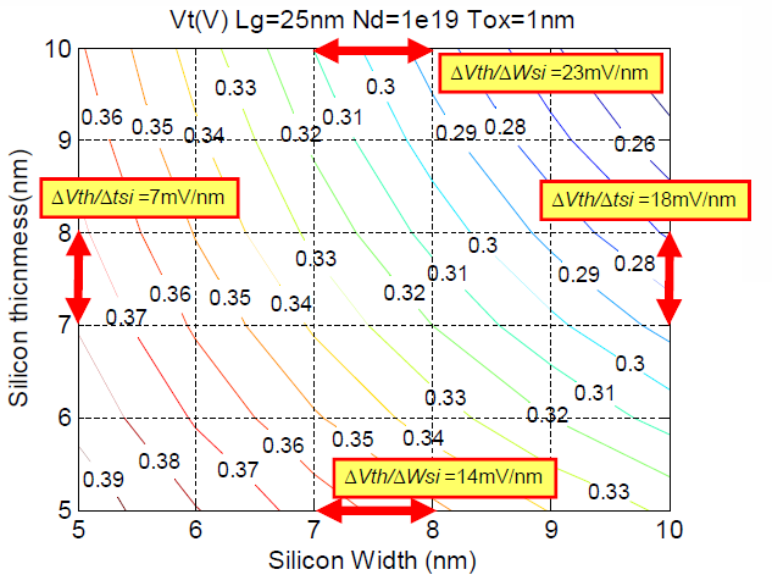
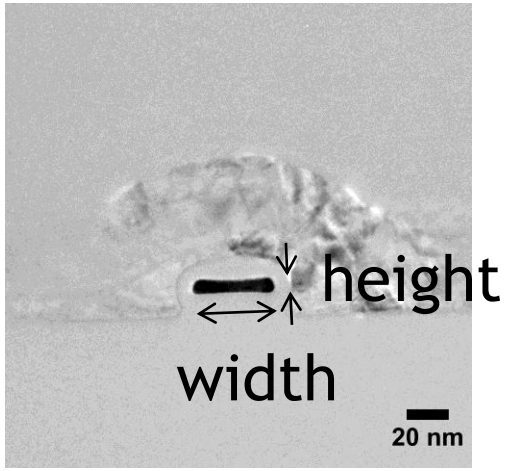
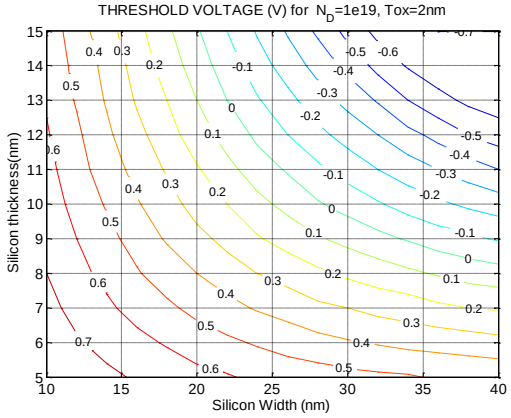
Process induced-Variability (1/3)



Process induced-Variability (2/3)



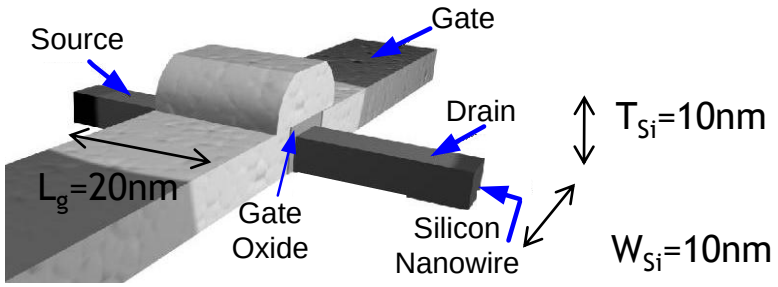


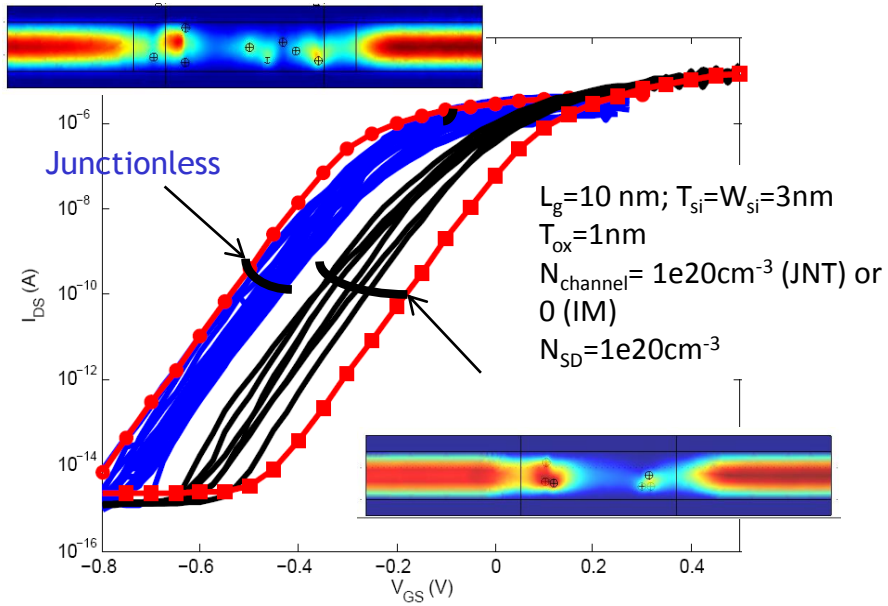


📖 A. Kranti. Junctionless nanowire transistor (JNT): Properties and design guidelines.
In: Proceedings of ESSDERC 2010, pp.357-360.

Process induced-Variability (3/3)

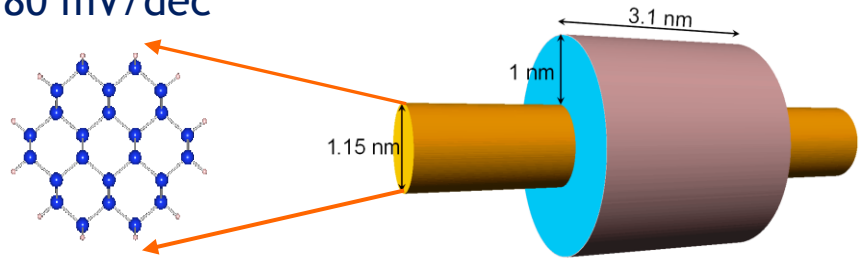
Doping concentration [cm^{-3}]	Statistical number of doping atoms in the channel
1e15	0.002
1e18	2
1e19	20





Conclusion

- Naturally CMOS-toolset compatible
- Switching properties:
  - SS=80mV/dec and DIBL=40 mV/V for JNT with L_g=25nm, W=25nm, T_{SOI}=10nm, V_d=0.9V (experimentally demonstrated by *CEA-LETI* within FP7-funded project *SQWIRE*)
- Scalability:
  - SS for p-channel JNT (L_g=3nm) is 80 mV/dec



- Manufacturability:
  - JNT suppress the difficulty of fabricating ultra-shallow junctions
  - SOI thickness control is critical

Acknowledgements

- Colleagues:
  - Prof. JP Colinge, N. Dehdashti Akhavan, P. Razavi, S. Das, R. Yu (*Ultimate Silicon Devices* Group);
  - N. Petkov, M. Schmidt (*Advanced Microscopy Facility* Group);
  - L. Ansari, G. Fagas, J. Greer (*Electronics Theory* Group)
  - Prof. G. Ghibaudo (INPG)

- Tyndall's Central Fabrication Facility

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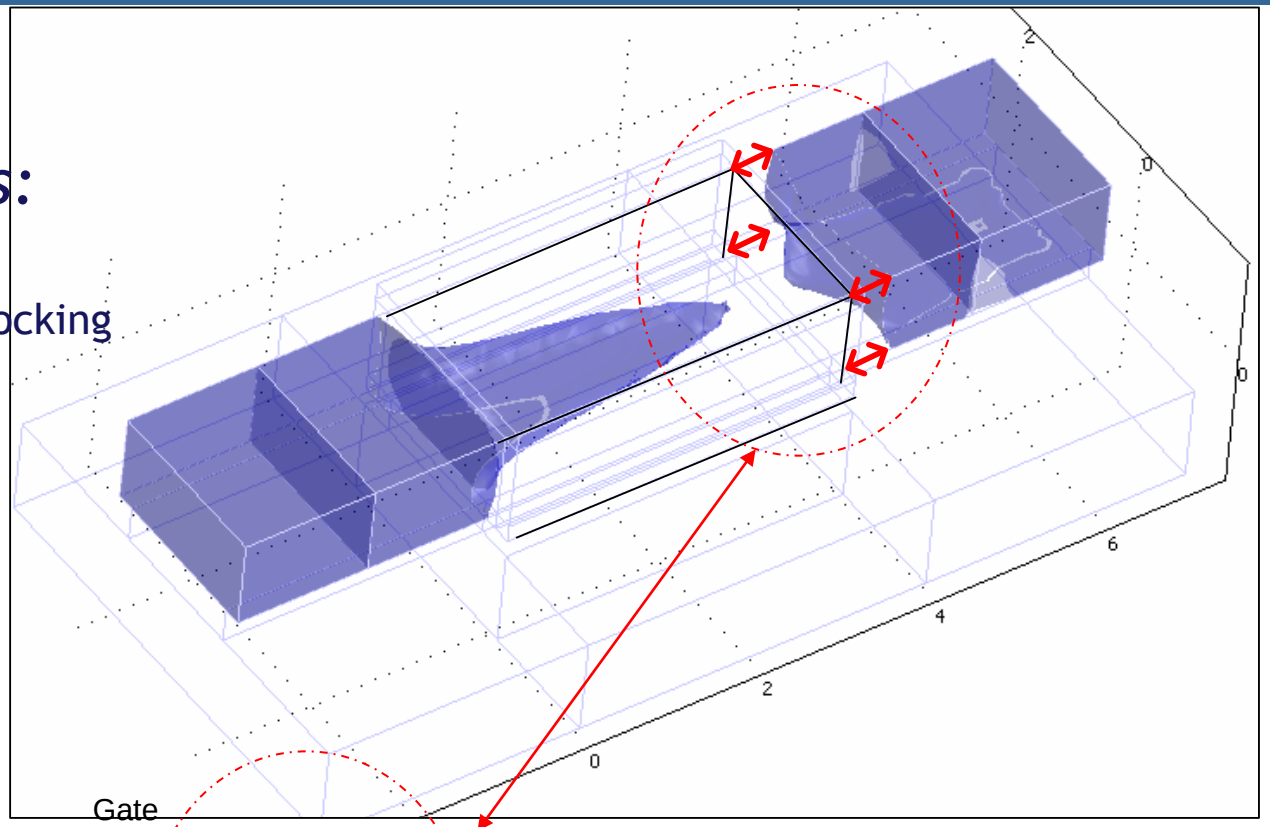
At High Gate Bias:

The saturation current-blocking region is *in the drain*, not in the channel region.



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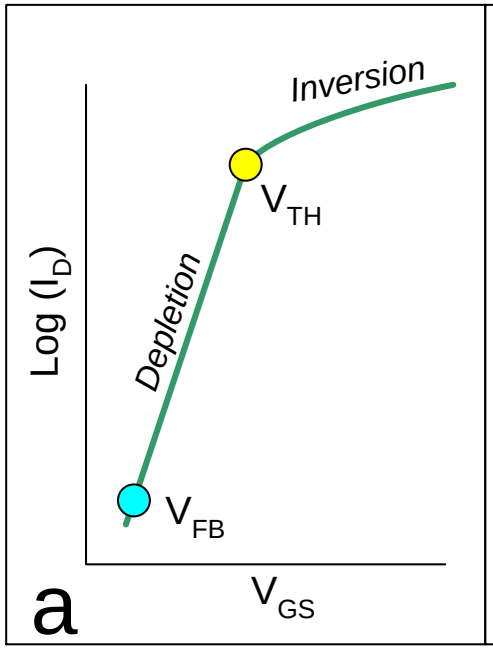
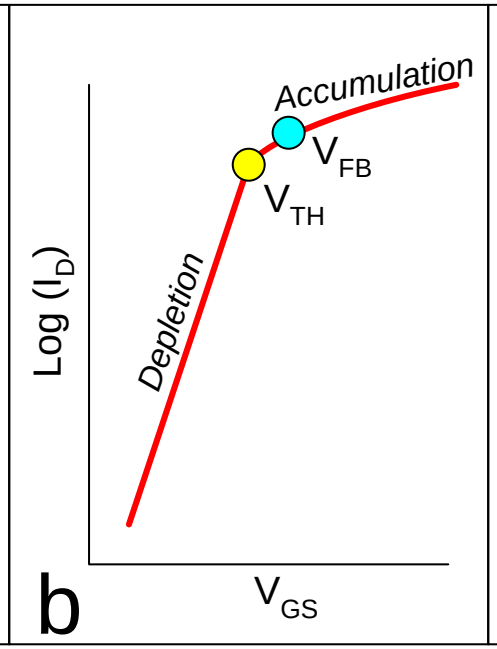
EUROPEAN REGIONAL DEVELOPMENT FUND

Inversion Mode



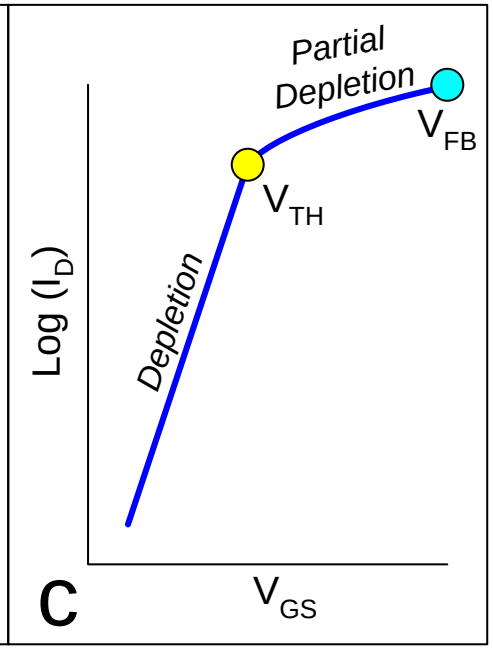
ON: Main Current in Surface Inversion Channels
OFF: Surface Subthreshold Current

Accumulation Mode



ON: Small body current & Surface Accumulation Channels
OFF: Body subthreshold current

Junctionless Mode



ON: Large body current
OFF: Body subthreshold current