Semiconducting Nanowire Platform for Autonomous Sensors

SiNAPS

Tyndall National Institute
(Coordinator)

Institut für Photonische Technologien e.V

École Polytechnique Fédérale de Lausanne

Imperial College of Science and Technology

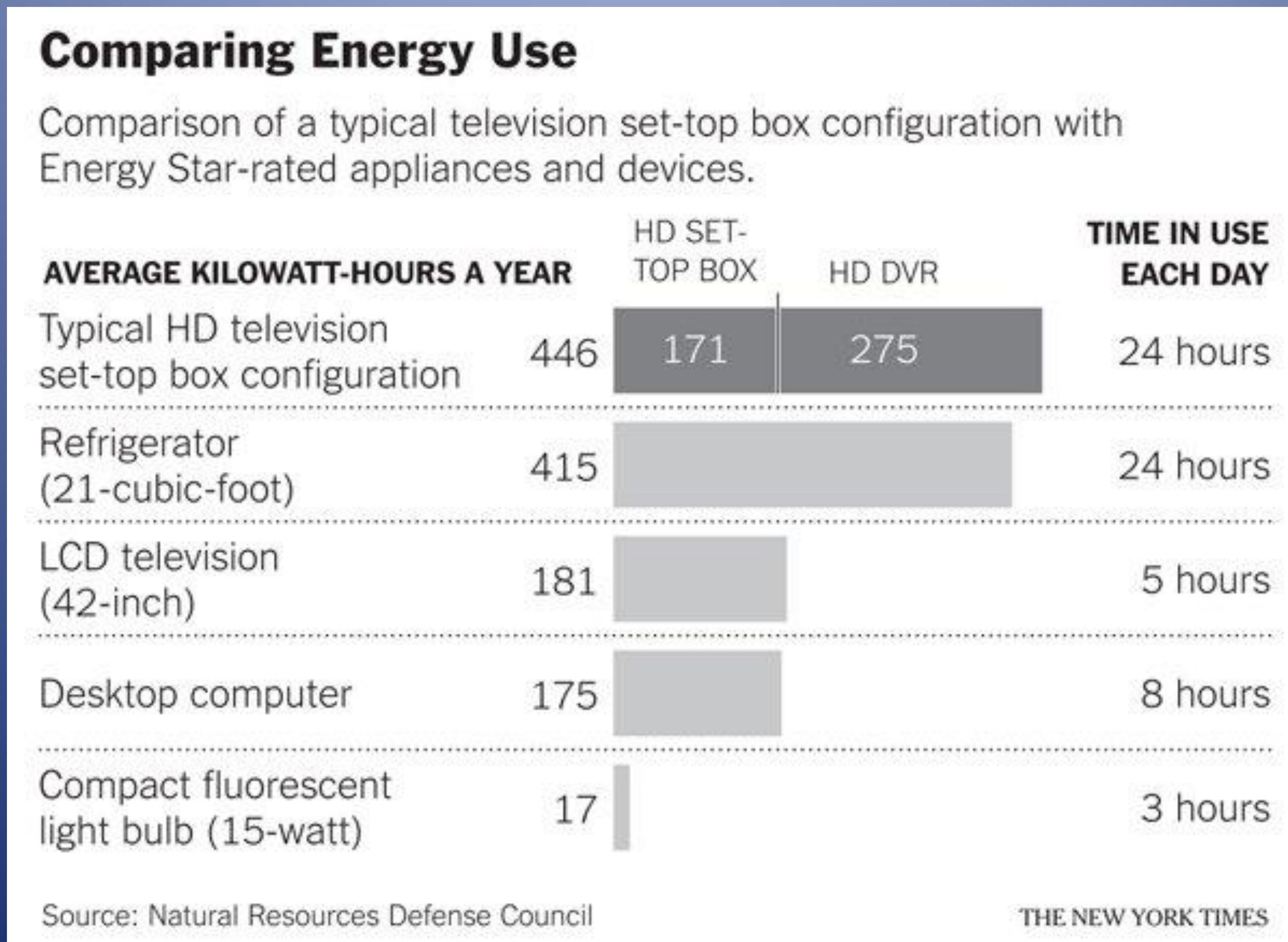
Aquamarijn Research BV

- Vision
- Project Objectives
- Highlights
- Impact

ICT energy pie grows fast

ICT and consumer electronics account for approximately 15% of global residential electricity consumption

Data: IEA report (2009)



1,700 TWh in two decades!

By 2030, energy use by household ICT and consumer electronics will triple consuming 1,700TWh

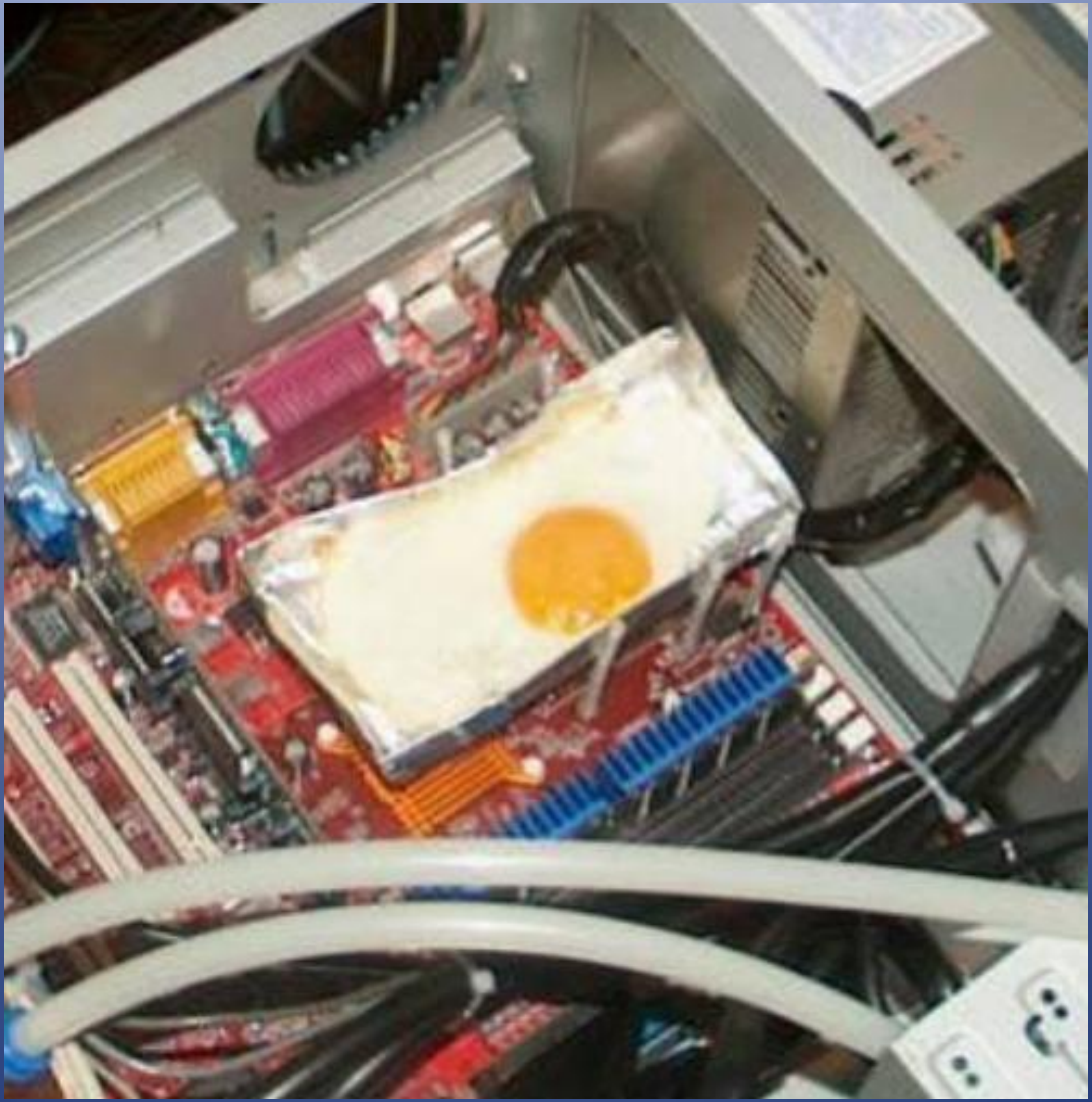
4,344 TWh

3,457 TWh

1,038 TWh

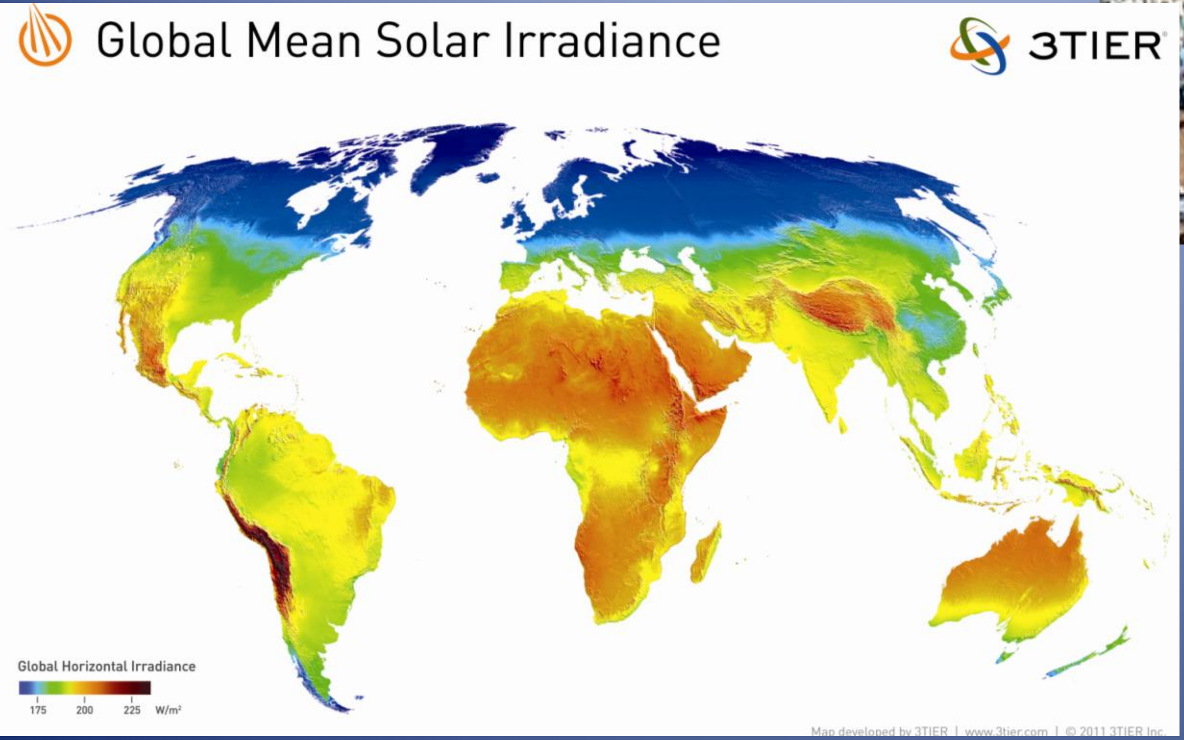
Maps: http://en.wikipedia.org
Data: IEA report (2010)

Reduce energy consumption per chip



Eric Pop group

Harvest ambient energy efficiently

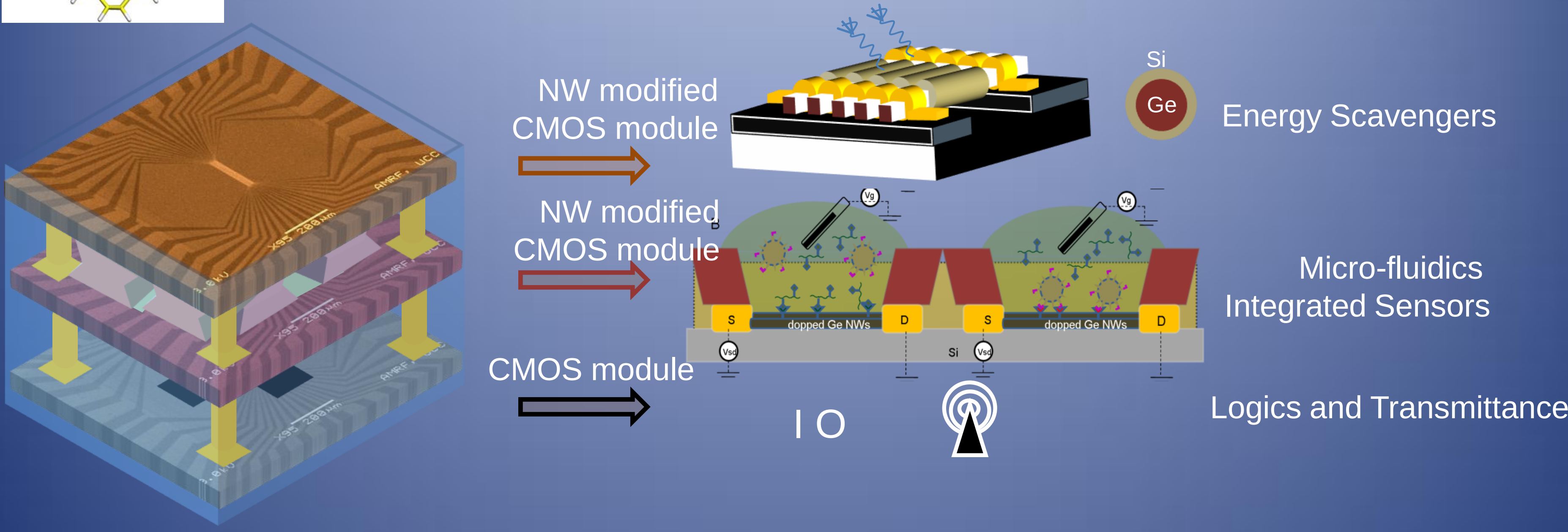


Images http://en.wikipedia.org

Manage efficiently power at the nano- and macro-scale

Utilise resources effectively

SiNAPS response



- A cost-effective technology enabling material platform
- Nanotech-based solar energy harvesting (generation II, III PVs)
- Energy-efficient ICT
- ICT for energy efficiency

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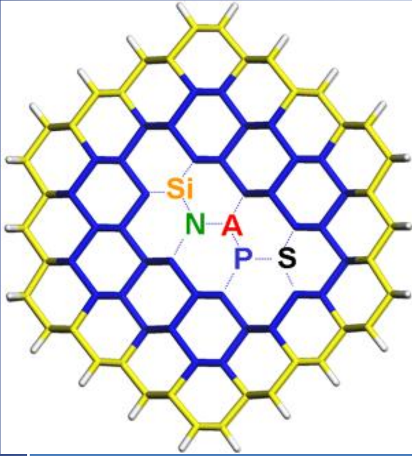
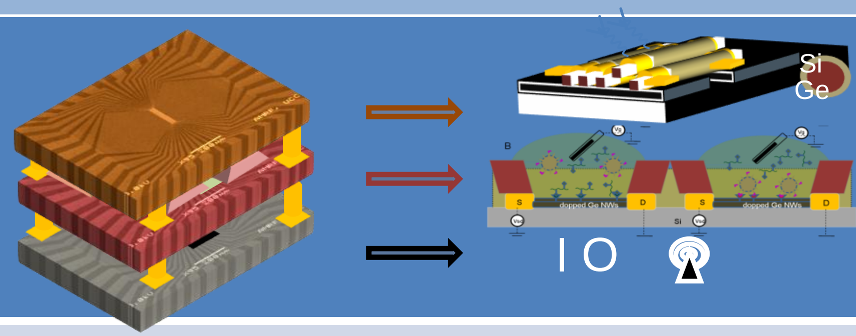


Science &Technology objectives



S&T1: Nanoscale energy harvesting system based on SiNWs

- develop core-shell semiconducting nanowires for efficient light absorption and charge separation
- fabricate high-efficiency PV mini-modules

S&T2: Power-efficient, highly-selective/sensitive NW-based chemical sensing

- develop surface functionalisation schemes on nanowires for selective binding
- demonstrate sensing of streptavidin using immobilised biotin

S&T3: Microfluidics for miniaturised nanowire-based chemical sensor

- develop a microfluidic delivery system to be integrated with the chemical nano-sensor.

S&T4: Efficient power management and data processing for micron-sized devices

- develop a low-power complete CMOS electronics sensing interface with an embedded energy management concept

S&T5: Integration into a single device of dimensions < 1mm^3

- integrate the individual modules into an Autonomous Platform with a target volume at and well beyond the state-of-the-art, namely, 4mm^3 and an ultimate target of smaller than 1 mm^3.

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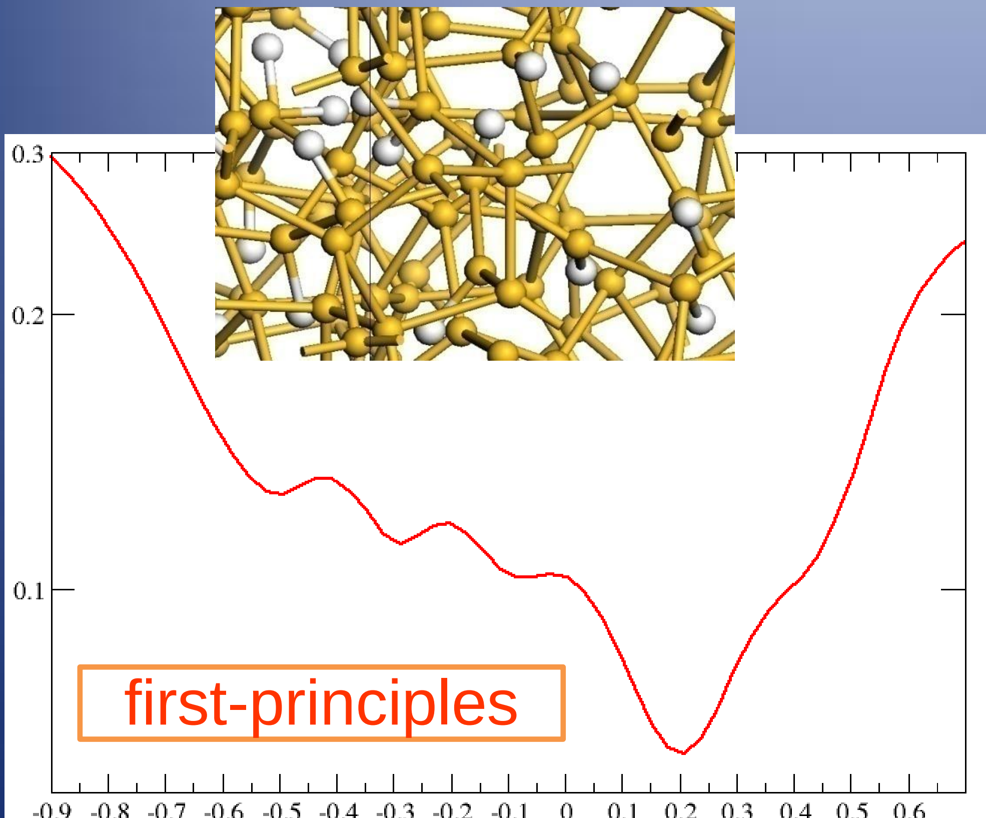
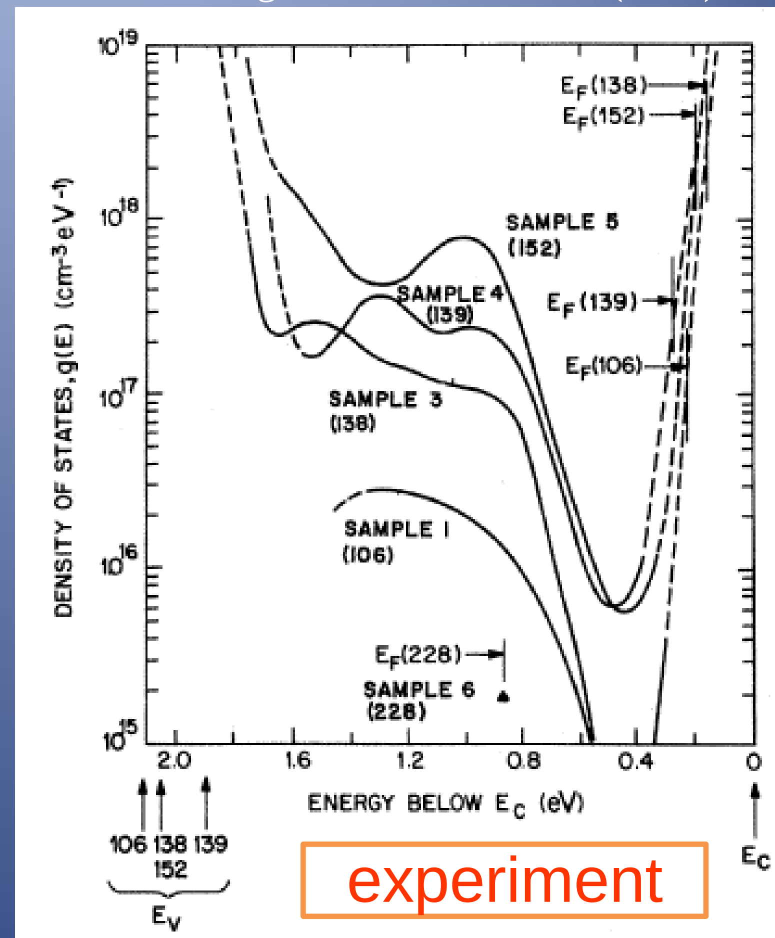
properties of a-Si:H from first-principles



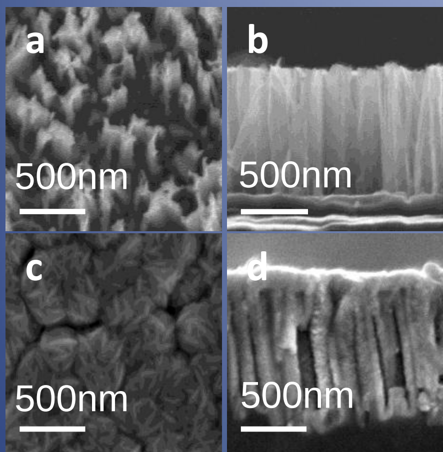
log of DOS vs energy (eV) for aSi:H (12%H)

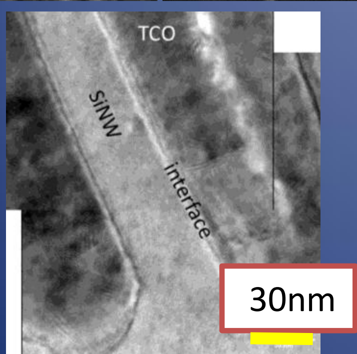
D.V. Lang et al, PRB 25, 5285 (1982)

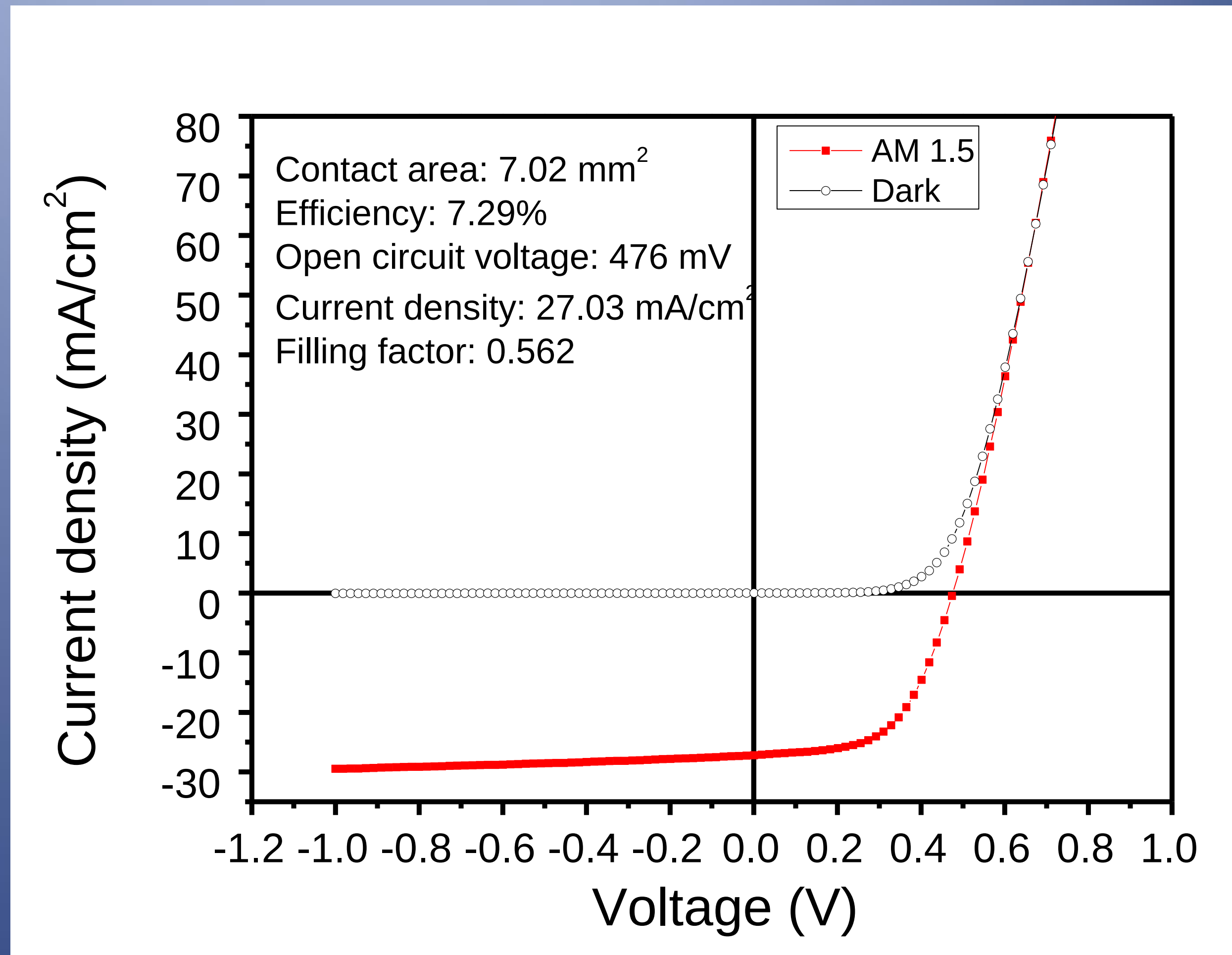


M. Legesse, M. Nolan and G. Fagas, unpublished

miniaturised solar cell with 7.29% efficiency

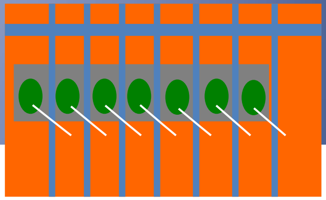


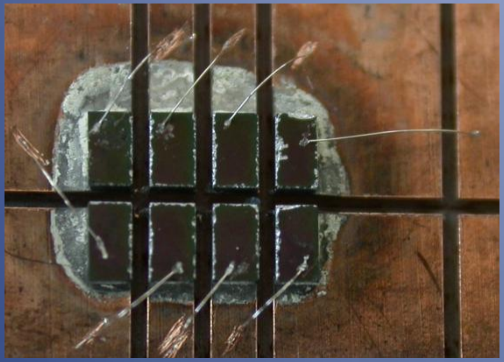


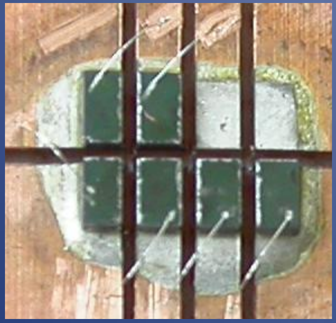


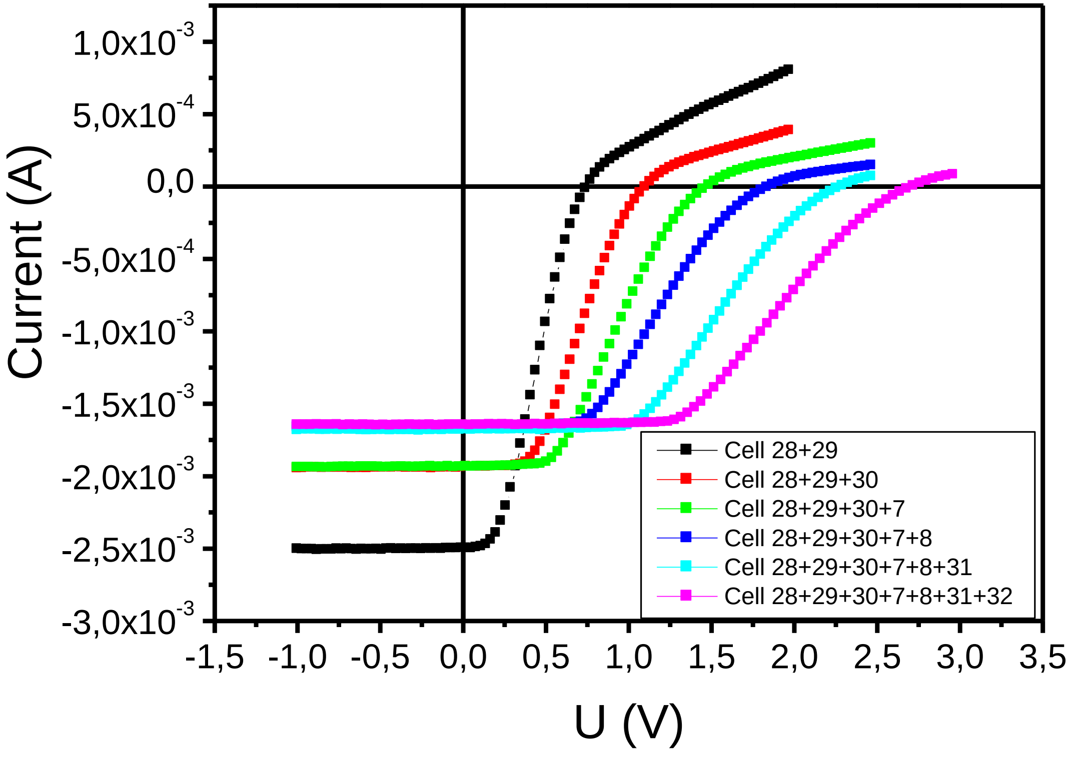
Guobin Jia, Martin Steglich, Ingo Sill, and Fritz Falk (IPHT), to appear in Solar Energy Materials and Solar Cells (2011)

PV mini-modules





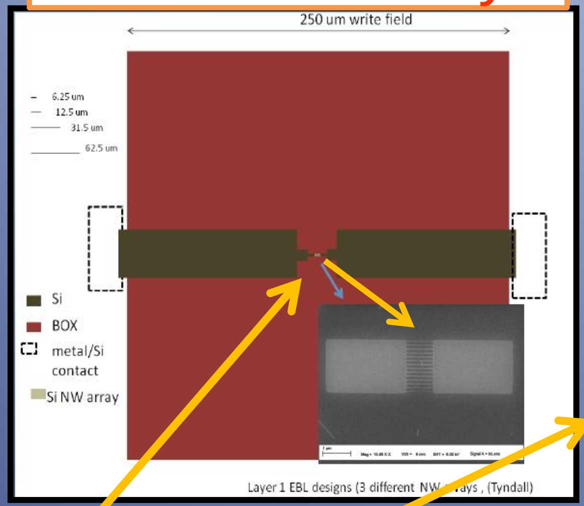




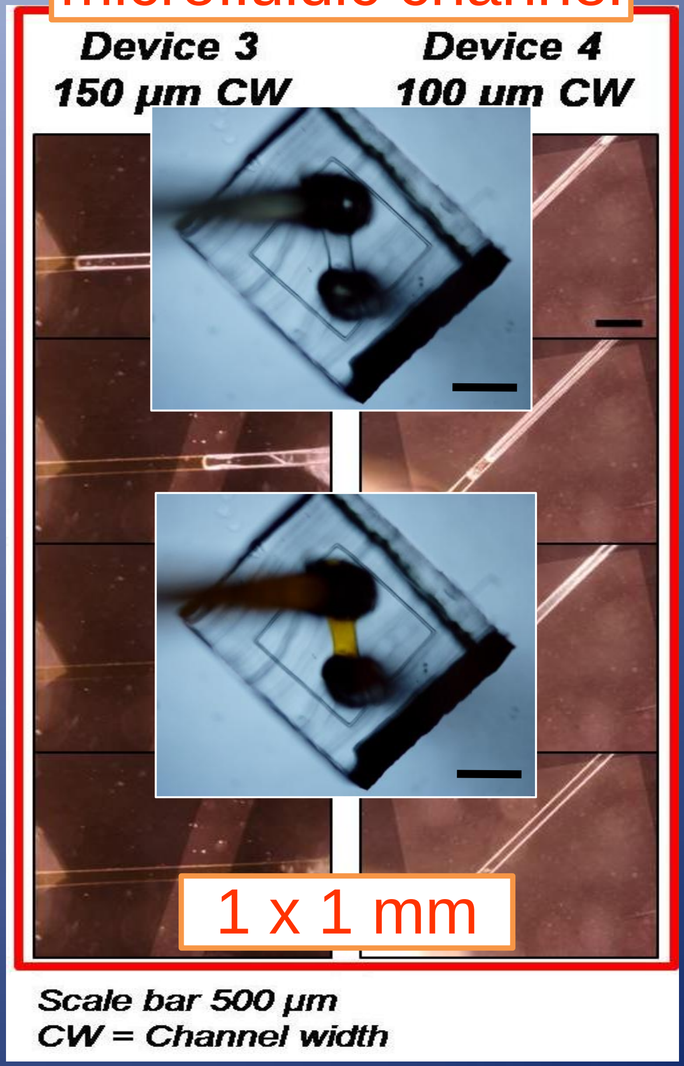
V_{OC}= 1.83 V
Active area ≈ 5.9 mm^2
P_{out} >150 µW

Miniaturised microfluidic delivery platform

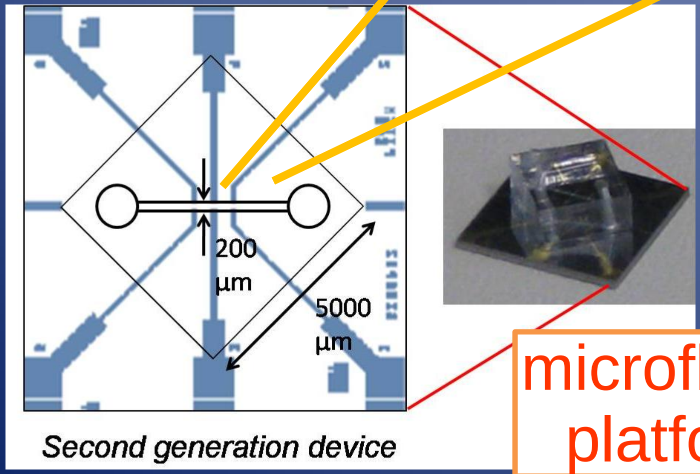
nanowire array



microfluidic channel

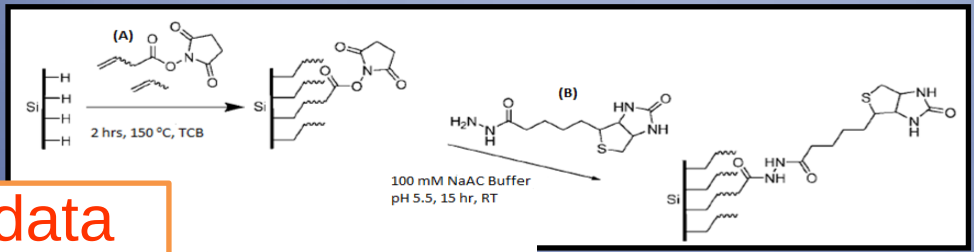


1 x 1 mm

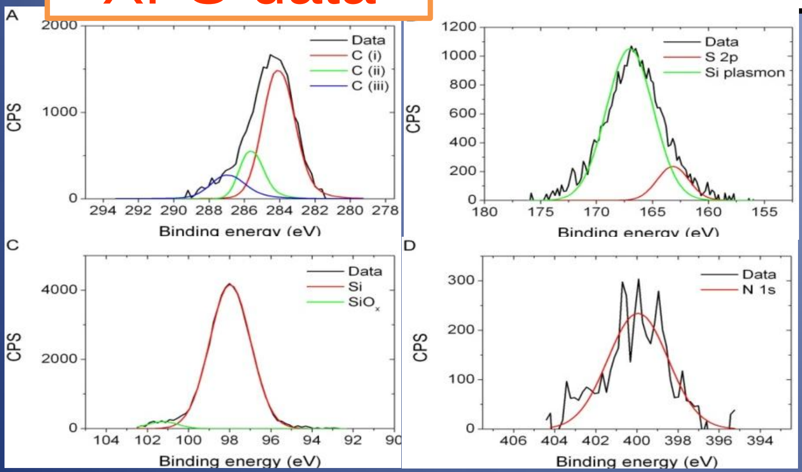


microfluidic platform

surface functionalisation demonstrating biotin-streptavidin binding

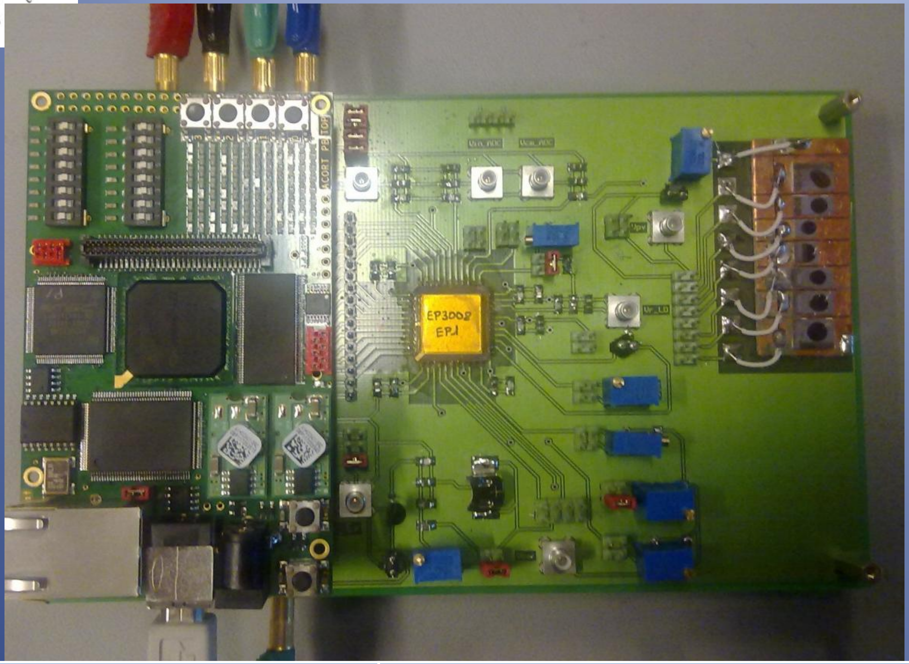


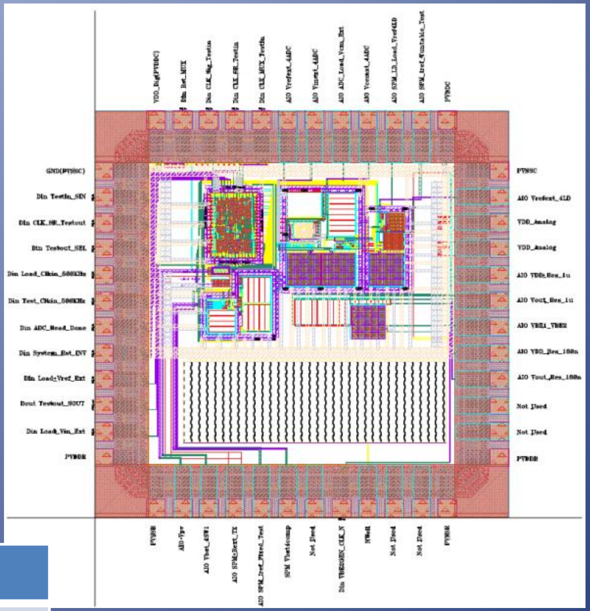
XPS-data



attached dye-conjugated streptavidin

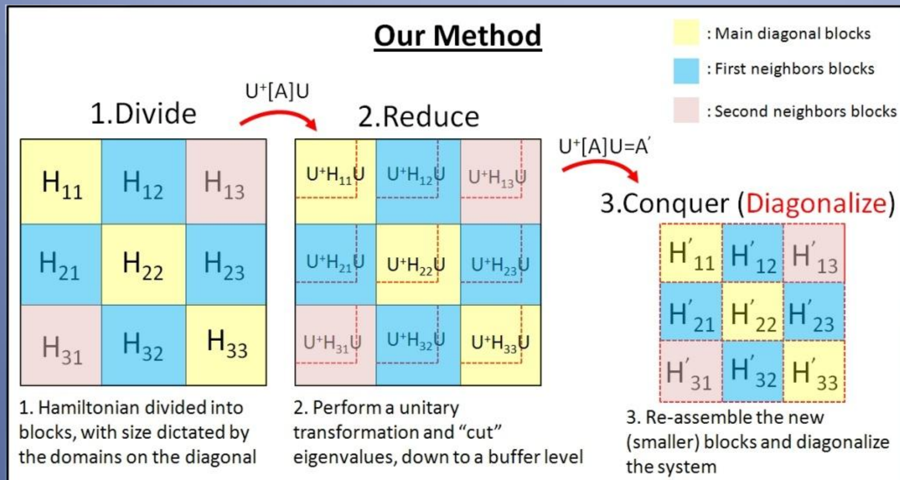
power management electronics



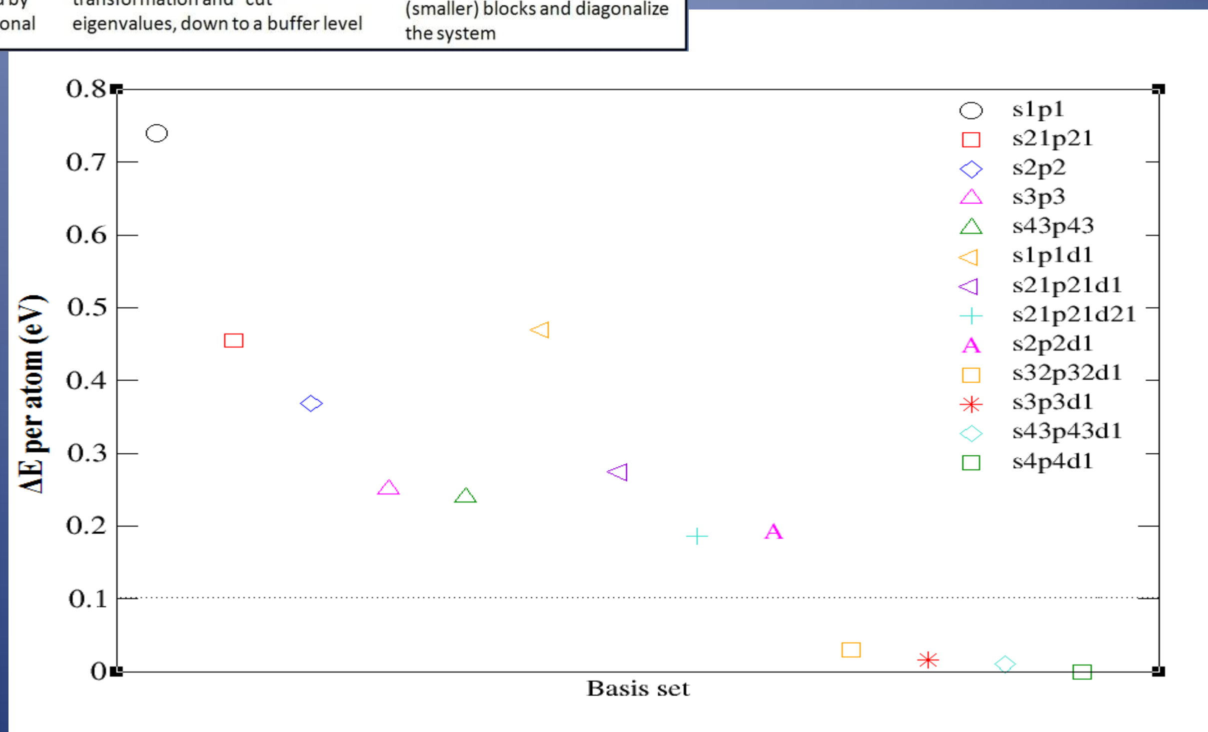


Specification	Value and/or Description
Main Chip Size	~ 500µmX700µm excl PADs inc test structures
Mini@sic Chip Area (including PADs)	1525X1525µm^2
Mini@sic Chip Area (without PADs)	1100X1100µm^2
Average Power Consumption (Power Management)	0.3µW
Average Power Consumption (Integrated Temperature Sensor)	2µW
Package	CLCC 44

fundamentals of efficient and accurate simulation tools



M. Iakovidis, GF
in preparation

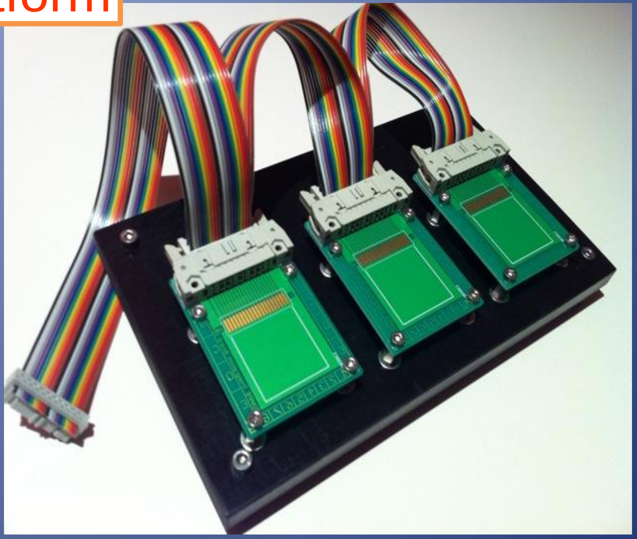


D. Sharma, H. Arefi, GF, *submitted*

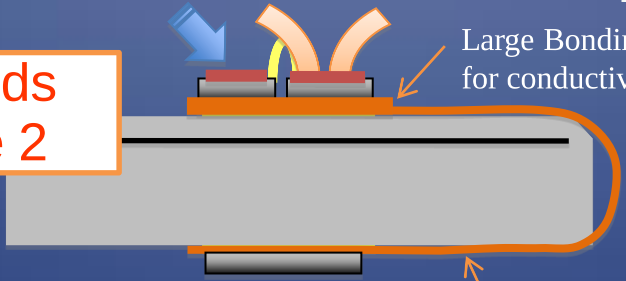
miniaturisation roadmap & integration

Issue1	Issue2	Issue3
Targets easy experimenting	Targets miniaturization while maintaining specifications	Targets miniaturization while losing minimal functionality
Test bed → helps with proof of principle	Proof of concept first SiNAPS Node	Proof of concept second SiNAPS Node
Chip size 25x25 [mm]	Chip size 2x2 [mm]	Chip size 1x1 [mm]
Integration based on PCB	Integration based on Polyimide or Ceramic substrate	Integration based on CMOS Die
Horizontal Single Substrate or Horizontal Multiple Substrate (depending on project phase)	Single Substrate with support for 3D integration with battery and radio	Single Substrate with support for 3D integration with battery and radio
Just intended for R&D testing	Target Date for Integration **M22**	Target Date for Integration **M30**

test platform



towards issue 2



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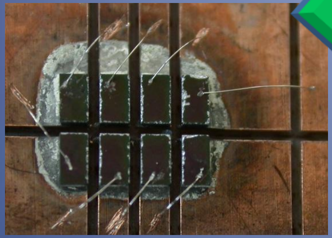
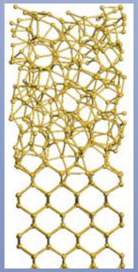
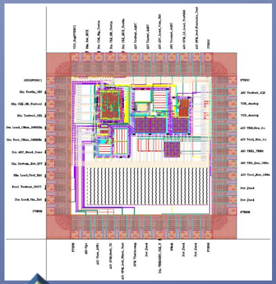
Innovation pathway





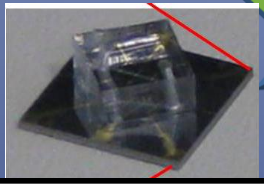
PV nanomaterial

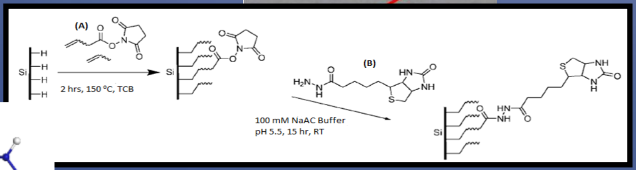
PMU and frontend co-design

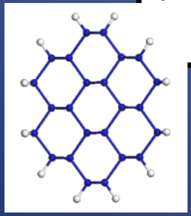


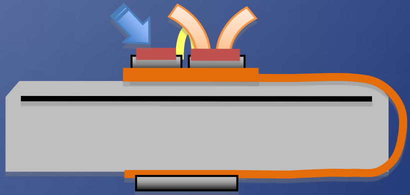
PV mini-modules

Chemical nanosensor









e-Health

Environment and Security

Energy

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SiNAPS

the team!