Welcome to the world of **JUNCTIONLESS NANOWIRE FETs!**

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Dimensions scaling
Dynamic power dissipation in present CMOS circuits at frequency, $f$, supply voltage, $V_{DD}$ and load capacitance $C_{load}$ can be described by:

$$P_{\text{dynamic}} = C_{load} \cdot V_{dd}^2 \cdot f_{\text{cycle}}$$

Any reduction of power consumption thus requires to reduce supply voltage.

$V_{dd}$ scaling is
- set by the threshold voltage of transistors
- dependent on the inverse sub-threshold slope ($kT/q$)
- limited by short-channel effects

→ Enhanced coupling between gate and channel

Courtesy: Prof. Gerard Ghibaudo (IMEP)
Enhanced Electrostatic Control

"1 Gate"

"2 Gates"

"3 Gates"

"Gate-all-Around"

"1 Gate" diagram:
- Gate
- Source
- Drain
- BOX

"2 Gates" diagram:
- Gate
- Source
- Drain
- Buried oxide

"3 Gates" diagram:
- Gate
- Source
- Drain
- Buried oxide

"Gate-all-Around" diagram:
- Gate
- Source
- Drain
- BOX

Text:
- Tri-Gate with 800°C 600Torr 5min H2 Anneal
- Fins are 45x78nm, Nice corner rounding by H2 anneal
- 20 nm
- Polysilicon Gate
- Silicon Fin
- Buried Oxide

Images:
- TEM images of gate, source, and drain regions.
Does it look too good to be true?

- Improved $L_g$ scalability
- Almost ideal sub-threshold slope (60mV/dec) at RT
- Low drain-to-source current ($I_{OFF}$)

- Drive current $I_{ON}$
  - crystal orientation dependence
  - High nano-wire pitch density
- Source/Drain resistance $R_{sd}$
  - SEG / Layout optimization needed

Critical Dimensions
- Gate length
- Gate oxide thickness
- Junction Depth

Critical Dimensions
- Nano-wire width
- Junction abruptness

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Junctionless nanowire transistors

DEVICE STRUCTURE
“Ultrashort channel” (<10nm)

Hooray!!
No need for source & drain engineering anymore!

The cross-section of the channel must be small enough so that the gate can deplete the heavily doped channel entirely (OFF state).
Junctionless nanowire transistors

CONDUCTION MECHANISM
**Electrostatic pinch-off:**

The cross section is small enough for the channel region to be depleted

\( V_D = 50 \text{mV}, \ N_d > 5 \times 10^{18} / \text{cm}^3 \)
Conduction mechanism (2/4)

- $V_D=50\text{mV}$
- $V_D=200\text{mV}$
- $V_D=400\text{mV}$
- $V_D=600\text{mV}$

$V_G > V_{TH}$

Channel pinch-off

$5x5 \ L_{\text{gate}}=10\text{nm}, \ t_{\text{ox}}=2\text{nm}$

- $V_{DS}=1.0\text{V}$
- $V_{DS}=50\text{mV}$

Drain Current (A)

Gate Voltage (V)

- DIBL: 48 mV, 66.2 mV/dec
- Junction-less: 48 mV, 66.2 mV/dec
- Inversion-mode: 153 mV, 83.8 mV/dec

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Channel in Multigate FETs @ $V_G = V_G = 1\text{V}$

$N^+PN^+$ Inversion Mode

$N_{\text{inv}} > 1 \times 10^{20}\text{ cm}^{-3}$

$N^+N^+N^+$ Junctionless $N_D = 1 \times 10^{19}\text{ cm}^{-3}$

Conduction mechanism (4/4)
Junctionless nanowire transistors

MOBILITY
**N⁺PN⁺ Inversion Mode**

$V_G = V_G = 1V$

$m_e = 50\text{ cm}^2/\text{Vs}$

Electric field $\sim 0\text{MV/cm}$ (flatband)

**N⁺N⁺N⁺ Junctionless**

$N_D = 1 \times 10^{19}\text{cm}^{-3}$

$m_e = 70\text{ cm}^2/\text{Vs}$

$m_e = 250\text{ cm}^2/\text{Vs}$

$m_e = 10\text{–}30\text{ cm}^2/\text{Vs}$

$V_G = V_G = 1V$

**Materials**

- SiO₂
- Silicon
- Conductor
- Electrodes
- \( L_g \) and EOT scaling \( \rightarrow \) increased \( E_{\text{eff}} \) in the channel \( \rightarrow \) \( \mu \) decreases

- Without strain technology the channel mobility in IM/AM FETs would be = or lower than in heavily doped Si

Junctionless nanowire transistors

PROCESS INDUCED-VARIABILITY
### Process induced-Variability (3/3)

<table>
<thead>
<tr>
<th>Doping concentration [cm(^{-3})]</th>
<th>Statistical number of doping atoms in the channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1e15</td>
<td>0.002</td>
</tr>
<tr>
<td>1e18</td>
<td>2</td>
</tr>
<tr>
<td>1e19</td>
<td>20</td>
</tr>
</tbody>
</table>

- **Source**
- **Drain**
- **Gate**
- **Silicon Nanowire**
- **Gate Oxide**

- \( T_{Si} = 10\text{nm} \)
- \( W_{Si} = 10\text{nm} \)

- Junctionless

\[
\begin{align*}
L_g &= 10\text{nm}; T_{si} = W_{si} = 3\text{nm} \\
T_{ox} &= 1\text{nm} \\
N_{\text{channel}} &= 1e20\text{cm}^{-3} \text{ (JNT) or 0 (IM)} \\
N_{SD} &= 1e20\text{cm}^{-3}
\end{align*}
\]
• Naturally CMOS-toolset compatible

• Switching properties:
  - $SS=80\text{mV/dec}$ and $DIBL=40\text{mV/V}$ for JNT with $L_g=25\text{nm}$, $W=25\text{nm}$, $T_{SOI}=10\text{nm}$, $V_d=0.9\text{V}$ (experimentally demonstrated by CEA-LETI within FP7-funded project SQWIRE)

• Scalability:
  - $SS$ for p-channel JNT ($L_g=3\text{nm}$) is $80\text{mV/dec}$

• Manufacturability:
  - JNT suppress the difficulty of fabricating ultra-shallow junctions
  - SOI thickness control is critical

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At High Gate Bias:

The saturation current-blocking region is *in the drain*, not in the channel region.
Annex 2

**Inversion Mode**

- **ON:** Main Current in Surface Inversion Channels
- **OFF:** Surface Subthreshold Current

**Accumulation Mode**

- **ON:** Small body current & Surface Accumulation Channels
- **OFF:** Body subthreshold current

**Junctionless Mode**

- **ON:** Large body current
- **OFF:** Body subthreshold current